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LOW-POWER SCHOTTKY TTL

This book presents technical data for a broad line of low-power Schottky TTL integrated circuits. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, the general characteristics and design considerations of this popular family are discussed, and selection guides are included to simplify the task of choosing the best combination of circuits for a system.

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Series A

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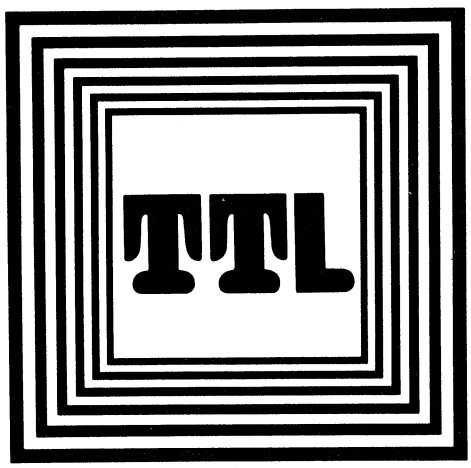
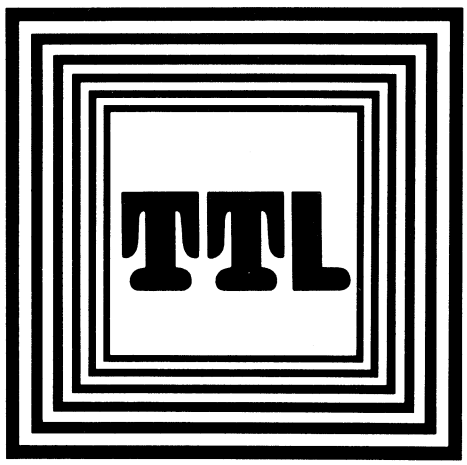


Introduction 1

LOW POWER SCHOTTKY



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INTRODUCTION

General Description – For many years TTL has been the most popular digital integrated circuit technology, offering a good compromise between cost, speed, power consumption and ease of use. As the price of TTL circuits decreased and the average IC complexity increased to MSI (medium scale integration), the cost and size of the power supply and the difficulty of removing the heat dissipated in the TTL circuits became increasingly important factors. Recent improvements in semiconductor processing have made it possible to not only reduce TTL power consumption significantly, but also to improve the speed over that of standard TTL.

LS Low Power Schottky TTL family combines a current and power reduction by a factor 5 (compared to 7400 TTL) with anti-saturation Schottky diode clamping and advanced processing, using shallower diffusions and higher sheet resistivity to achieve circuit performance better than conventional TTL. With a full complement of popular TTL functions available in LS, Low Power Schottky is destined to become the dominating TTL logic family.

LS represents more than just a conventional speed versus power trade-off. This is best illustrated by *Figure 1* which compares LS to other TTL technologies. Note that LS dissipates eleven times less power than S or 74S, suffering a delay increase of only 1.7 times.

To the system designer the advantages of this new TTL family are many:

- Less supply current allows smaller, cheaper power supplies, reducing equipment cost, size and weight.
- Lower power consumption means less heat is generated, which simplifies thermal design. Packing density can be increased or cooling requirements reduced, or perhaps both. The number of cooling fans can be reduced, or slower, quieter ones substituted.
- Reliability is enhanced, since lower dissipation causes less chip temperature rise above ambient; lower junction temperature increases MTBF. Also, lower chip current densities minimizes metal related failure mechanisms.
- Less noise is generated, since the improved transistors and lower operating currents lead to much smaller current spikes than standard TTL, which means that fewer or smaller power supply decoupling capacitors are needed. In addition, load currents are only 25% of standard TTL and 20% of HTTL, which means that when a logic transition occurs that current changes along signal lines are proportionately smaller, as are the changes in ground current. Rise and fall times, and thus wiring rules, are the same as for standard TTL and more relaxed than for HTTL or STTL.
- Simplified MOS to TTL interfacing is provided, since the input load current of LSTTL is only 25% of a standard TTL load.
- Ideally suited for CMOS to TTL interfacing, CMOS and most other 4000 or 74C CMOS are designed to drive one LS input load at 5.0 V. The LS can also interface directly with CMOS operating up to 15 V due to the high voltage Schottky input diodes.
- Best TTL to MOS or CMOS driver. With the modest input current of MOS or CMOS as a load, any LS output will rise up to within 1 V of V_{CC}, and can be pulled up to 10 V with an external resistor.
- Interfaces directly with other TTL types, as indicated in the input and output loading tables.
- The functions and pinouts are the same as the familiar 7400/9300 series, which means that no extensive learning period is required to become adept in their use.

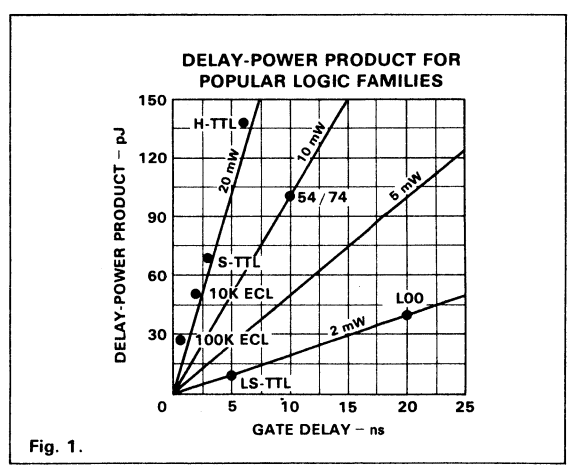


Fig. 1.

Circuit Characteristics

The LS circuit features are easiest explaned by using the LS00 2-input NAND gate as an example. The input/output circuits of all LS TTL, including, SSI, MSI are almost identical. While the logic function and the basic structure of LS circuits are the same as conventional TTL, there are also significant differences, as explained below:

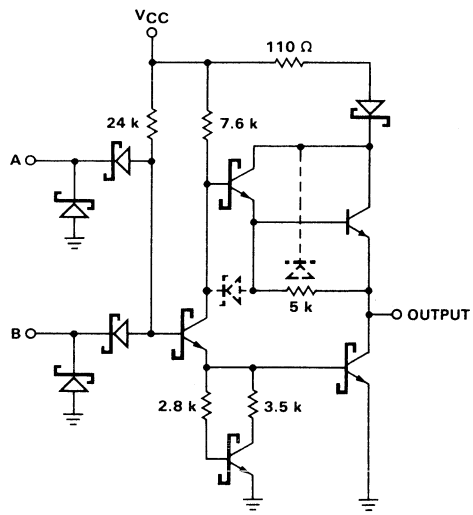


Fig. 2.

Input Configuration

LSTTL is considered part of the TTL family, but it does not use the multi-emitter input structure that originally gave TTL its name. All LS TTL, with the exception of some early designs, employ a DTL-type input circuit which uses Schottky diodes to perform the AND function. Compared to the classical multi-emitter structure, this circuit is faster and it increases the input breakdown voltage to 15 V. Each input has a Schottky clamping diode which conducts when an input signal goes negative, as indicated by the input characteristic of *Figure 3.* This helps to simplify interfacing with those MOS circuits whose output signal tends to go negative. For a long TTL interconnection, which acts like a transmission line, the clamp diode acts as a termination for a negative-going signal and thus minimizes ringing. Otherwise, ringing could become significant when the finite delay along an interconnection is greater than one-fourth the fall time of the driving signal.

The effective capacitance of an LSTTL input is approximately 3.3 pF. For an input which serves more than one internal function, each additional function adds 1.5 pF.

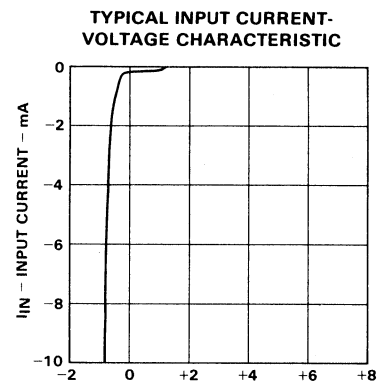


Fig. 3.

Output Configuration

The output circuits of Low Power Schottky TTL have several features not found in conventional TTL. A few of these features are discussed below.

- The base of the pull-down output transistor is returned to ground through a resistor-transistor network instead of through a simple resistor. This squares up the transfer characteristics since it prevents conduction in the phase-splitter until base current is supplied to the pull-down output transistor. This also improves the propagation delay and transition time. *(See Figure 4)*

- The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5 kΩ resistor to the output terminal. (Unlike 74H and 74S where it is returned to ground, which is a more power consuming configuration). This configuration allows the output to pull-up to one V_{BE} below V_{CC} for low values of output current.

- As a unique feature, the LS outputs use a Schottky diode in series with the Darlington collector resistor. This diode allows the output to be pulled substantially higher than V_{CC} (e.g., to +10 V, convenient for interfacing with CMOS). For the same reason the parasistic diode of the base return resistor is connected to the Darlington common collector, not to V_{CC}. Some early LS designs – the LS00, 02, 04, 10, 11, 20, 32, 74, 109, 112, 113, and 114 – do not have the diode in series with the Darlington collector resistor. These outputs are, therefore, clamped one diode drop above the positive supply voltage (V_{CC}). These older circuits also contain a "speed-up" diode that supplies additional phase splitter current while the output goes from HIGH to LOW and also limits the maximum output voltage to one diode drop above V_{CC}. Since this is the fastest transition even without additional speed-up, this diode is omitted in all new designs.

Output Characteristics

Figure 5 shows the LOW state output characteristics. For low I_{OL} values, the pull-down transistor is clamped out of deep saturation which contributes to speed. The curves also show the clamping effect when I_{OL} tends to go negative, as it often does due to reflections on a long interconnection after a negative-going transition. This clamping effect helps to minimize ringing.

The waveform of a rising output signal resembles an exponential, except that the signal is slightly rounded at the beginning of the rise. Once past this initial rounded portion, the starting edge rate is approximately 0.5 V/ns with a 15 pF load and 0.25 V/ns with a 50 pF load. For analytical purposes, the rising waveform can be approximated by the following expression.

$$v(t) = V_{OL} + 3.7\,[1 - \exp(-t/T)]$$

where

$T = 8$ ns for $C_L = 15$ pF

$= 16$ ns for $C_L = 50$ pF

The waveform of a falling output signal resembles that part of a cosine wave between angles of 0° and 180°. Fall times from 90% to 10% are approximately 4.5 ns with a 15 pF load and 8.5 ns with a 50 pF load. Equivalent edge rates are approximately 0.8 V/ns and 0.4 V/ns, respectively. For analytical purposes, the falling waveform can be approximated by the following expression.

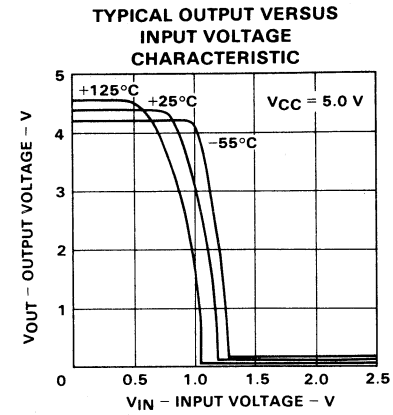


Fig. 4.

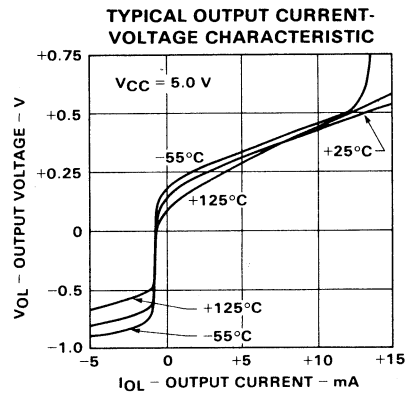


Fig. 5.

$$v(t) = V_{OL} + 1.9\,\mu(t)\,[1 + \cos \omega t] - 1.9\,\mu(t-a)\,[1 + \cos \omega(t-a)]$$

where

$\mu(t) = 0$ for $t < 0$
$= 1$ for $t > 0$

and

$\mu(t-a) = 0$ for $t < a$
$= 1$ for $t > a$

For t in nanoseconds and $C_L = 15$ pF,

$a = 7.5$ ns, $\omega = 0.42$

For $C_L = 50$ pF,

$a = 14$ ns, $\omega = 0.23$

AC Switching Characteristics

The average propagation delay of a Low Power Schottky gate is 5 ns at a load of 15 pF as shown in *Figure 6*. The delay times increase at an average of 0.08 ns/pF for larger values of capacitance load. These delay times are relatively insensitive to variations in power supply and temperature. The average propagation delay time changes less than 1.0 ns over temperature and less than 0.5 ns with V_{CC} for the military temperature and voltage ranges. (See *Figures 8* and *9*).

The power versus frequency characteristics of the LS family, as shown in *Figure 7*, indicate that at operating frequencies above 1 MHz the Low Power Schottky devices are more efficient than CMOS for most applications.

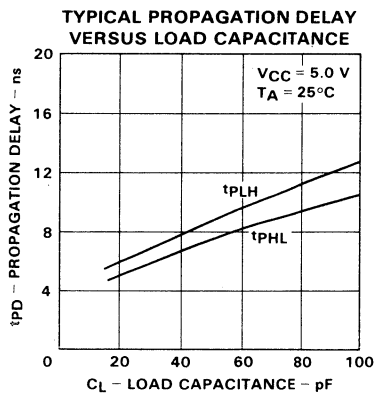


Fig. 6.

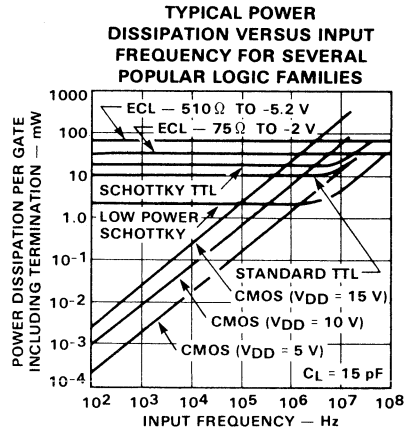


Fig. 7.

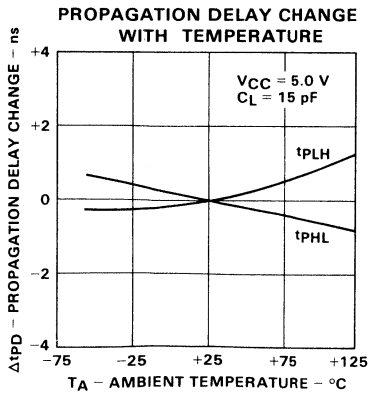


Fig. 8.

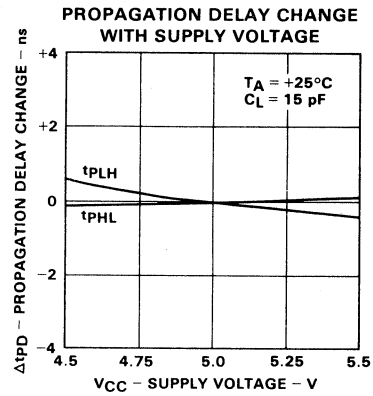


Fig. 9.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET

CURRENTS – Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply current** – The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

I_{IH} **Input HIGH current** – The current flowing into an input when a specified HIGH voltage is applied.

I_{IL} **Input LOW current** – The current flowing out of an input when a specified LOW voltage is applied.

I_{OH} **Output HIGH current** – The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OL} **Output LOW current** – The current flowing into an output which is in the LOW state.

I_{OS} **Output short circuit current** – The current flowing out of an output which is in the HIGH state when that output is short circuited to ground (or other specified potential).

I_{OZH} **Output off current HIGH** – The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

I_{OZL} **Output off current LOW** – The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

VOLTAGES – All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.,* −10 V is greater than −1.0 V).

V_{CC} **Supply voltage** – The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

$V_{CD(MAX)}$ **Input clamp diode voltage** – The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.

V_{IH} **Input HIGH voltage** – The range of input voltages that represents a logic HIGH in the system.

$V_{IH(MIN)}$ **Minimum input HIGH voltage** – The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} **Input LOW voltage** – The range of input voltages that represents a logic LOW in the system.

$V_{IL(MAX)}$ **Maximum input LOW voltage** – The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

$V_{OH(MIN)}$ **Output HIGH voltage** – The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

$V_{OL(MAX)}$ **Output LOW voltage** – The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET (Cont'd)

V_{T+} **Positive-going threshold voltage** – The input voltage of a variable threshold device (*i.e.,* Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.

V_{T-} **Negative-going threshold voltage** – The input voltage of a variable threshold device (*i.e.,* Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$.

AC SWITCHING PARAMETERS

f_{MAX} **Toggle frequency/operating frequency** – The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_W **Pulse width** – The time between 1.3 V amplitude points on the leading and trailing edges of a pulse.

t_h **Hold time** – The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s **Set-up time** – The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} **Output disable time (of a 3-state output) from HIGH level** – The time between the 1.3 V level on the input and a voltage 0.5 V below the steady state output HIGH level with the 3-state output changing from the defined HIGH level to a high-impedance (off) state.

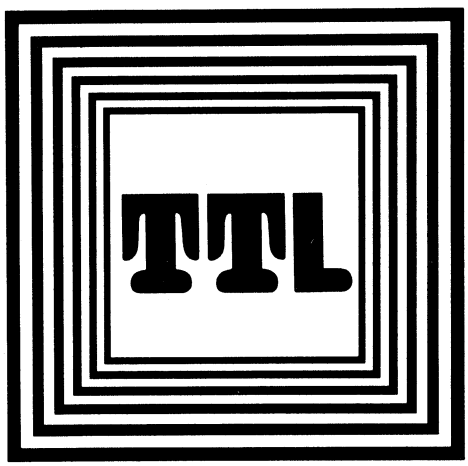
t_{PLZ} **Output disable time (of a 3-state output) from LOW level** – The time between the 1.3 V level on the input and a voltage 0.5 V above the steady state output LOW level with the 3-state output changing from the defined LOW level to a high-impedance (off) state.

t_{PZH} **Output enable time (of a 3-state output) to a HIGH level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a HIGH level.

t_{PZL} **Output enable time (of a 3-state output) to a LOW level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a LOW level.

t_{rec} **Recovery time** – The time between the 1.3 V level on the trailing edge of an asynchronous input control pulse and the 1.3 V level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

LOW POWER SCHOTTKY



Design Considerations 2

2

DESIGN CONSIDERATIONS

Supply Voltage and Temperature Range
The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0 V. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250 mV) over an ambient temperature range of 0°C to 75°C. MIL-grade parts are guaranteed to perform with a ±10% supply tolerance (±500 mV) over an ambient temperature range of −55°C to +125°C.

TTL families may be mixed for optimum system design. The following tables specify the worst case noise immunity in mixed systems.

Worst Case TTL DC Noise Immunity / Noise Margins

Electrical Characteristics

Item	Symbol	Motorola TTL Families	Military (−55 to +125°C)				Commercial (0 to 75°C)				Units
			V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
6	TTL	Standard TTL (54/74)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
7	HTTL	High Speed TTL (54H/74H)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
8	LPTTL	Low Power TTL, L00 (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
9	STTL	Schottky TTL (54S/74S), 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
10	LSTTL	Low Power Schottky TTL (54LS/74LS)	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

V_{OL} and V_{OH} are the voltages generated at the output. V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate output levels. The numbers given above are guaranteed worst-case values.

LOW Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	300	400	300	mV
HTTL	400	400	300	400	300	mV
LPTTL	500	500	400	500	400	mV
STTL	300	300	200	300	200	mV
LSTTL	400	400	300	400	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	500	500	500	500	500	mV
LSTTL	500	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

LOW Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	500	500	500	500	500	mV
STTL	300	300	300	300	300	mV
LSTTL	300	300	300	300	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	700	700	700	700	700	mV
LSTTL	700	700	700	700	700	mV

From "V_{OH}" to "V_{IH}"

Fan-in and Fan-out

In order to simplify designing with Motorola TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40 μA
in the HIGH state (logic "1")

1 TTL Unit Load (U.L.) = 1.6 mA
in the LOW state (logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

EXAMPLES—INPUT LOAD

1. A 7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)
2. The 74LS95 which has a value of I_{IL} = 0.8 mA and I_{IH} of 40 μA on the CP terminal, is specified as having an input LOW load factor of

$$\frac{0.8\ mA}{1.6\ mA} \text{ or } 0.5 \text{ U.L.}$$

and an input HIGH load factor of

$$\frac{40\ \mu A}{40\ \mu A} \text{ or } 1 \text{ U.L.}$$

3. The 74LS00 gate which has an I_{IL} of 0.36 mA and an I_{IH} of 20 μA, has an input LOW load factor of

$$\frac{0.36\ mA}{1.6\ mA} \text{ or } 0.225 \text{ U.L.}$$

(normally rounded to 0.25 U.L.) and an input HIGH load factor of

$$\frac{20\ \mu A}{40\ \mu A} \text{ or } 0.5 \text{ U.L.}$$

EXAMPLES—OUTPUT DRIVE

1. The output of the 7400 will sink 16 mA in the LOW (logic "0") state and source 800 μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore

$$\frac{16\ mA}{1.6\ mA} = 10 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{800\ \mu A}{40\ \mu A} \text{ or } 20 \text{ U.L.}$$

2. The output of the 74LS00 (Commercial Grade) will sink 8.0 mA in the LOW state and source 400 μA in the HIGH state. The normalized output LOW drive factor is

$$\frac{8.0\ mA}{1.6\ mA} \text{ or } 5 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{400\ \mu A}{40\ \mu A} \text{ or } 10 \text{ U.L.}$$

Relative load and drive factors for the basic TTL families are given in *Table I*.

TABLE I

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

Wired-OR Applications

Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between a maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(LOW) \bullet 1.6\ mA}$$

$$R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \bullet I_{OH} + N_2(HIGH) \bullet 40\ \mu A}$$

where:

R_X = External Pull-up Resistor
N_1 = Number of Wired-OR Outputs
N_2 = Number of Input Unit Loads being Driven
$I_{OH} = I_{CEX}$ = Output HIGH Leakage Current
I_{OL} = LOW Level Fan-out Current of Driving Element
V_{OL} = Output LOW Voltage Level (0.5 V)
V_{OH} = Output HIGH Voltage Level (2.4 V)
V_{CC} = Power Supply Voltage

Example: Four 74LS03 gate outputs driving four other 74LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25\ V - 0.5\ V}{8\ mA - 1.6\ mA} = \frac{4.75\ V}{6.4\ mA} = 742\ \Omega$$

$$R_{X(MAX)} = \frac{4.75\ V - 2.4\ V}{4 \bullet 100\ \mu A + 2 \bullet 40\ \mu A} = \frac{2.35\ V}{0.48\ mA} = 4.9\ k\Omega$$

where:

N_1 = 4
$N_2(HIGH)$ = 4 • 0.5 U.L. = 2 U.L.
$N_2(LOW)$ = 4 • 0.25 U.L. = 1 U.L.
I_{OH} = 100 μA
I_{OL} = 8 mA
V_{OL} = 0.5 V
V_{OH} = 2.4 V

Any value of pull-up resistor between 742 Ω and 4.9 kΩ can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

Unused Inputs

For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

1. Connect unused input to V_{CC}. Most 74LS inputs have a breakdown voltage $>$ 15 V and require, therefore, no series resistor. For all multi-emitter conventional TTL inputs, a 1 to 10 kΩ current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

2. Connect the unused input to the output of an unused gate that is forced HIGH.

CAUTION: Do not connect an unused LSTTL input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.

Interconnection Delays

For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes with STTL to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 150 Ω to 200 Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, *e.g.,* if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

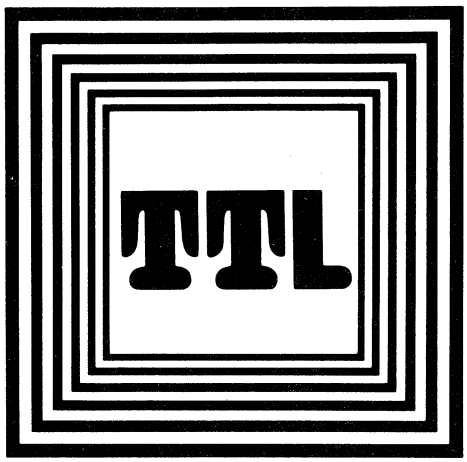
If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-cast situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

Another advantage of LSTTL has to do with its output impedance during a positive-going transition. Whereas the low output impedance of STTL and HTTL allows these circuits to force a larger initial swing into a low impedance interconnection, the low output impedance also has a disadvantage. It makes the reflection coefficient negative at the driven end of the interconnection, a circumstance that exists any time a transmission line is terminated by an impedance lower than its characteristic impedance. This means that when the reflection from the (essentially) open end of the interconnection arrives back at the driver it will be re-reflected with the opposite polarity. The result is a sequence of reflected signals which alternate in sign and decrease in magnitude, commonly known as ringing. The lower the driver output impedance, the greater the amplitude of the ringing and the longer it takes to damp out.

The output impedance of LSTTL, on the other hand, is closer to the characteristic impedance of the interconnections commonly used with TTL, and ringing is practically non-existent. Thus no special packaging is required. This advantage, combined with excellent speed, modest edge rates and very low transient currents, are some of the reasons that designers have found LSTTL extremely easy to work with and very cost effective.

LOW POWER SCHOTTKY



Device Index and Selector Information

3

NUMERICAL INDEX OF DEVICES

NUMERICAL INDEX OF DEVICES (Cont'd)

DEVICES TO BE INTRODUCED

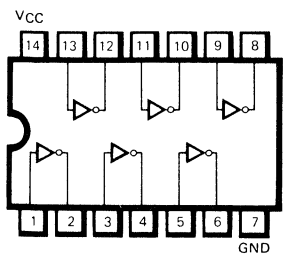
DEVICE	DESCRIPTION
SN54LS01/SN74LS01	Quad 2-Input NAND Gate (Open Collector)
SN54LS12/SN74LS12	Triple 3-Input NAND Gate (Open Collector)
SN54LS13/SN74LS13	Dual 4-Input Schmitt Trigger
SN54LS26/SN74LS26	Quad 2-Input NAND (Open Collector 15 V)
SN54LS28/SN74LS28	Quad 2-Input NOR Buffer
SN54LS33/SN74LS33	Quad 2-Input NOR Buffer (Open Collector)
SN54LS75/SN74LS75	Quad Transparent Latch
SN54LS76/SN74LS76	Dual JK Flip-Flop
SN54LS77/SN74LS77	Quad Transparent Latch
SN54LS78/SN74LS78	Dual JK Flip-Flop
SN54LS85/SN74LS85	4-Bit Magnitude Comparator
SN54LS89/SN74LS89	16 x 4 RAM
SN54LS107/SN74LS107	Dual JK Flip-Flop
SN54LS165/SN74LS165	8-Bit Parallel In/Serial Out Shift Register
SN54LS168/SN74LS168	Up/Down Decade Counter
SN54LS169/SN74LS169	Up/Down Binary Counter
SN54LS173/SN74LS173	4-Bit D Register (3-State)
SN54LS257/SN74LS257	Quad 2-Input Multiplexer (3-State)
SN54LS260/SN74LS260	Dual 5-Input NOR Gate
SN54LS273/SN74LS273	Octal D Flip-Flop w/Master Reset (20-Pin)
SN54LS280/SN74LS280	9-Bit Parity Generator/Checker
SN54LS352/SN74LS352	Dual 4-Input Multiplexer (Inverting LS153)
SN54LS353/SN74LS353	Dual 4-Input Multiplexer (3-State)
SN54LS373/SN74LS373	Octal Transparent Latch (20-Pin)
SN54LS377/SN74LS377	Octal D Flip-Flop w/Enable
SN54LS378/SN74LS378	Hex D Flip-Flop w/Enable
SN54LS379/SN74LS379	4-Bit D Flip-Flop w/Enable
SN54LS390/SN74LS390	Dual Decade Counter
SN54LS393/SN74LS393	Dual 4-Bit Binary Counter
SN54LS395/SN74LS395	4-Bit Shift Register 3-State MIL-DEC
SN54LS490/SN74LS490	Dual Decade Counter

SSI SELECTOR GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol	LSTTL Data Sheet Page No.
NAND Gates						
Hex Inverters	54/74LS04	54/7404	54/74H04	54/74S04	D-1	4-6
Hex Inverts (O.C.)	54/74LS05	54/7405	54/74H05	54/74S05	D-1	4-7
Hex Schmitt Trigger	54/74LS14	54/7414			D-1	4-12
Quad 2-Input	54/74LS00	54/7400	54/74H00	54/74S00	D-2	4-3
Quad 2-Input (O.C.)	54/74LS03	54/7403	54/74H01	54/74S03	D-2	4-5
Quad 2-Input (48 mA)	54/74LS37	54/7437			D-2	4-21
Quad 2-Input (O.C. 48 mA)	54/74LS138	54/7438			D-2	4-22
Quad 2-Input Schmitt	54/74LS132	54/74132		54/74S132	D-2	4-42
Triple 3-Input	54/74S10	54/7410	54/74H10	54/74S10	D-3	4-10
Dual 4-Input	54/74LS20	54/7420	54/74H20	54/74S20	D-4	4-15
Dual 4-Input (O.C.)	54/74LS22	54/7422	54/74H22	54/74S22	D-4	4-17
Dual 4-Input Buffer	54/74LS40	54/7440	54/74H40	54/74S40	D-4	4-23
8-Input	54/74LS30	54/7430	54/74H30	54/74S30	D-5	4-19
NOR Gates						
Quad 2-Input	54/74LS02	54/7402		54/74S02	D-6	4-4

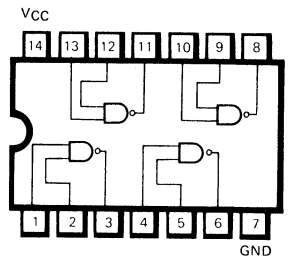
SSI LOGIC SYMBOLS

D1



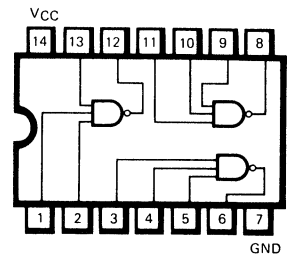
LS04, LS05, LS14

D2



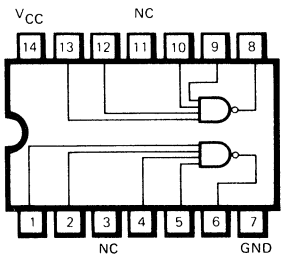
LS00, LS03, LS37
LS38, LS132

D3



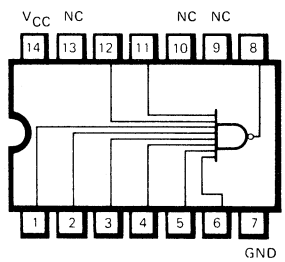
LS10

D4



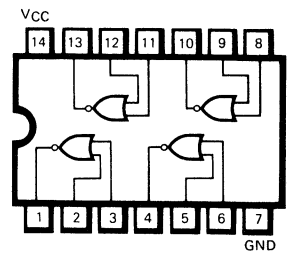
LS20, LS22,
LS40

D5



LS30

D6



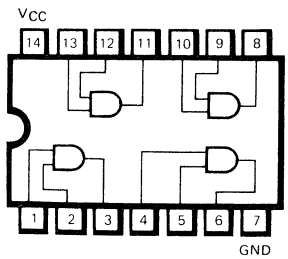
LS02

SSI SELECTOR GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol	LSTTL Data Sheet Page No.
AND Gates						
Quad 2-Input	54/74S08	54/7408	54/74H08	54/74S08	D-7	4-8
Quad 2-Input (O.C.)	54/74LS09	54/7409	54/74H09	54/74S09	D-7	4-9
Triple 3-Input	54/74LS11	54/7411	54/74H11	54/74S11	D-8	4-11
Triple 3-Input (O.C.)	54/74S15		54/74H15	54/74S15	D-8	4-14
Dual 4-Input	54/74LS21	54/7421	54/74H21		D-9	4-16
OR Gates						
Quad 2-Input	54/74LS32	54/7432		54/74S32	D-10	4-20
Exclusive OR Gate						
Quad 2-Input	54/74LS86	54/7486		54/74S86	D-11	4-31
Quad 2-Input (O.C)	54/74LS136				D-11	4-45
Exclusive NOR Gate						
Quad 2-Input (O.C.)	54/74LS266	8242			D-12	4-46
AND-OR-INVERT Gates						
Dual 2-2 Input	54/74LS51	54/7451	54/74H51	54/74S51	D-13	4-24
2-2-3-3 Input	54/74LS54				D-14	4-25
4-4 Input	54/74LS55				D-15	4-26

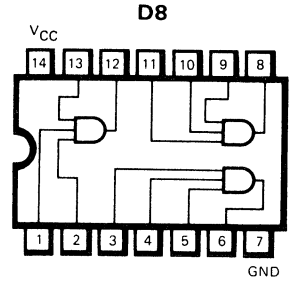
SSI LOGIC SYMBOLS

D7



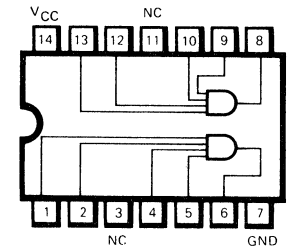
LS08, LS09

D8



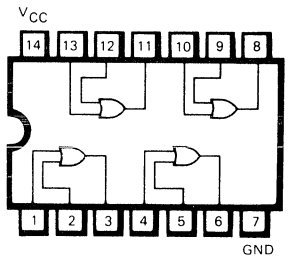
LS11, LS15

D9



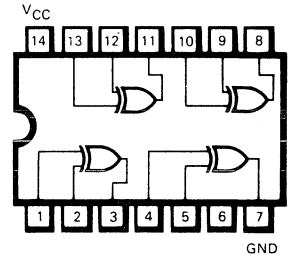
LS21

D10



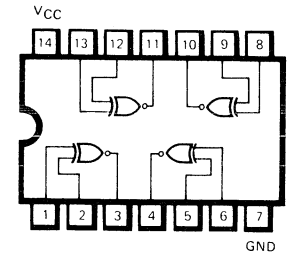
LS32

D11



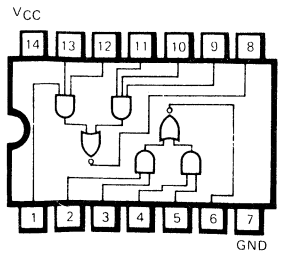
LS86, LS136

D12



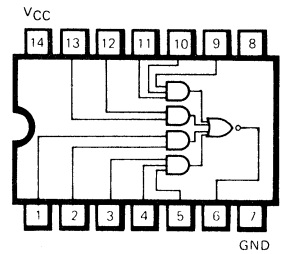
LS266

D13



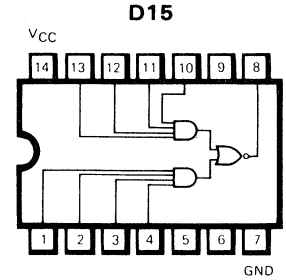
LS51

D14



LS54

D15



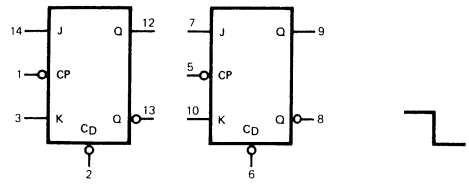
LS55

SSI SELECTOR GUIDE

Function	Low Power Schottky 5 ns/2 mW	Std. TTL 54/74 10 ns/10 mW	High Speed 54/74H 6 ns/22 mW	High Speed Schottky 3 ns/19 mW	Logic Symbol	LSTTL Data Sheet Page No.
Dual Flip-Flops						
Dual JK	54/74LS73	54/7473	55/74H73, 54/74H103		D-16	4-27
Dual D	54/74LS74	54/7474	54/74H74	54/74S74	D-17	4-29
Dual J$\overline{K}$	54/74LS109	54/74109		54/74S109	D-18	4-32
Dual JK	54/74LS112			54/74S112	D-19	4-34
Dual JK	54/74LS113			54/74S113	D-20	4-36
Dual JK	54/74LS114			54/74S114	D-21	4-38

SSI FLIP-FLOP LOGIC DIAGRAM

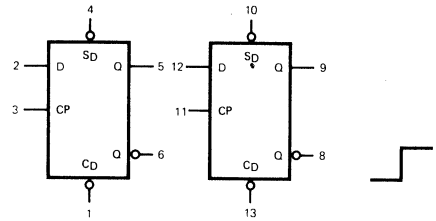
D16



V_{CC} = Pin 4
GND = Pin 11

LS73

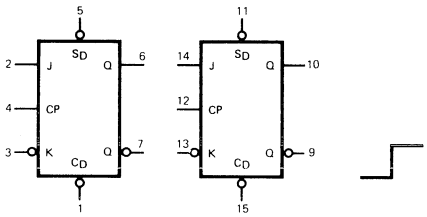
D17



V_{CC} = Pin 14
GND = Pin 7

LS74

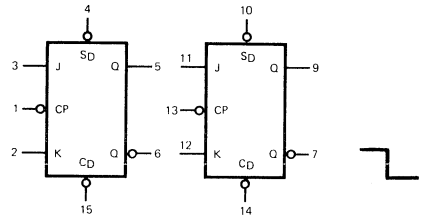
D18



V_{CC} = Pin 16
GND = Pin 8

LS109

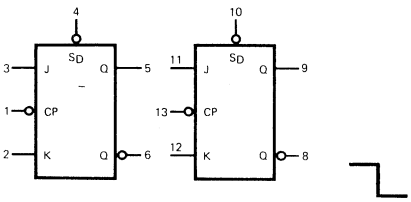
D19



V_{CC} = Pin 16
GND = Pin 8

LS112

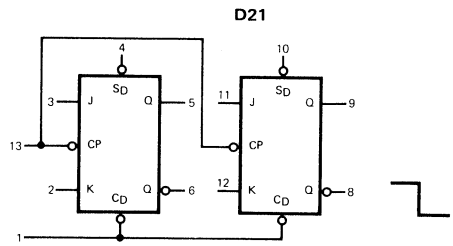
D20



V_{CC} = Pin 14
GND = Pin 7

LS113

D21



V_{CC} = Pin 14
GND = Pin 7

LS114

MSI SELECTOR GUIDE BY FUNCTION

Arithmetic Operators
(CLA = Carry Lookahead)

Function	DEVICE NO.	Description	No. of Bits	t_{pd} ns	Power Dissipation mW (typ)	LSTTL Data Sheet Page No.
Adder	74LS83	Full Binary 4-Bit w/Carry	4	15	95	5-6
Adder	74LS283	Full Binary 4-Bit w/Carry	4	15	95	5-109
Arithmetic Logic Unit	74LS181	ALU with External CLA	4	20	105	5-63

MSI SELECTOR GUIDE BY FUNCTION

Counters

A = Asynchronous S = Synchronous

Function	DEVICE NO	Modulo	Parallel Load	Clock Transition	Max Clock Rate MHz (typ)	Clock to Q Output Delay ns (typ)	Power Dissipation mW (typ)	LSTTL Data Sheet Page No.
Asynchronous	74LS90	2x5		⌝	50	33	45	5-9
Asynchronous	74LS92	2x6		⌝	50	33	45	5-9
Asynchronous	74LS93	2x8		⌝	50	46	45	5-9
Asynchronous	74LS196	2x5	A	⌝	60	48	60	5-89
Asynchronous	74LS197	2x8	A	⌝	70	60	60	5-89
Synchronous	74LS160	10 Presettable	S	⌟	45	15	95	5-44
Synchronous	74LS161	16 Presettable	S	⌟	45	15	95	5-44
Synchronous	74LS162	10 Presettable	S	⌟	45	15	95	5-44
Synchronous	74LS163	16 Presettable	S	⌟	45	15	95	5-44
Up / Down	74LS192	10	A	⌟	40	30	85	5-75
Up / Down	74LS193	16	A	⌟	40	30	85	5-75
Up / Down	74LS190	10	A	⌟	40	20	90	5-68
Up / Down	74LS191	16	A	⌟	40	20	90	5-68

MSI SELECTOR GUIDE BY FUNCTION

Decoders/Demultiplexers

Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

Function	DEVICE NO.	Address Inputs	Active LOW Enable	Active LOW Outputs	Open Collector Output Voltage	Address Delay ns (typ)	Enable Delay ns (typ)	Power Dissipation mW (typ)	Fan-out (UL)	LSTTL Data Sheet Page No.
Dual 1-of-4	74LS139	2+2	1+1	4+4		22	19	34	5	5-22
Dual 1-of-4	74LS155	2	2+2	4+4		18	15	30	5	5-34
Dual 1-of-4	74LS156	2	2+2	4+4	5.5 V	33	26	31	5	5-34
1-Of-8	74LS259	3	1	8		30	19	60	5	5-108
1-of-8	74LS42	3	1	8		17	17	35	5	5-3
1-of-8	74LS138	3	3	8		22	21	34	5	5-19
1-of-10	74LS42	4 (BCD)		10		17		35	5	5-3

MSI SELECTOR GUIDE BY FUNCTION

Latches/Flip-Flops

Function	DEVICE NO.	Data Inputs	Common Clear	Enable/Clock Inputs (Level)	Required Enable/Clock Pulse Width ns (typ)	Enable/Clock to Q Delay ns (typ)	Data to Q Delay ns (typ)	Power Dissipation mW (typ)	LSTTL Data Sheet Page No.
4-Bit R-S Latch	74LS279	4x(RS)	-	-	-	-	14	19	4-47
4-Bit D Latch	74LS197	4xD	L	1(L)	20	28	24	60	5-89
4-Bit D Latch	74LS197	4xD	L	1(L)	20	28	24	60	5-89
4-Bit D Flip-Flop	74LS175	4xD	L	1(⎍)	20	21	-	55	5-60
4-Bit D Flip-Flop	74LS298	4x2	-	1(⎍)	20	20	-	65	5-121
6-Bit D Flip-Flop	74LS174	6	L	1(⎍)	20	21	-	80	5-57
8-Bit Add. Latch	74LS259	1xD	L	1(L) 3 add. bits	11	18	28	70	5-108
4x4 Register File	74LS170	4xD	-	2	25	-	26	125	5-53
4x4 Register File (3-state)	74LS670	4xD	-	2	25	-	24	150	5-124

MSI SELECTOR GUIDE BY FUNCTION

Multiplexers

Unit Load (UL) = 40 μA HIGH/1.6 mA LOW

Function	DEVICE NO.	Enable Inputs	True Output	Complement Output	Select Delay ns (typ)	Enable Delay ns (typ)	Data Delay ns (typ)	Power Dissipation mW (typ)	Fan-Out (UL)	LSTTL Data Sheet Page No.
Quad 2-Input	74LS157	1	X		18	14	9	49	5	5-38
Quad 2-Input	74LS158	1		X	16	12	7	24	5	5-41
Quad 2-Input	74LS257	1	3-State		14	16	12	50	5	5-102
Quad 2-Input	74LS258	1		3-State	12	16	10	35	5	5-105
Quad 2-Input	74LS298	Clocked (edge-trigger)	X Latched		-	20	-	65	5	5-121
Dual 4-Input	74LS153	2	X		18	16	10	31	5	5-31
Dual 4-Input	74LS253	2	3-State		18	16	10	43	5	5-99
8-Input	74LS151	1	X	X	28	25	18	30	5	5-25
8-Input	74LS251	1	3-State	3-State	29	21	18	33	5	5-95
8-Input	74LS152			X	22	-	11	28	5	5-28

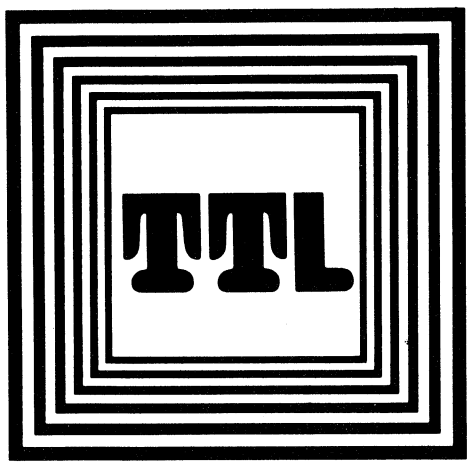
MSI SELECTOR GUIDE BY FUNCTION

Registers

A = Asynchronous S = Synchronous

Function	DEVICE NO.	No. of Bits	Serial Entry	Parallel Entry No. of Bits	Clock Edge	Max Clock Freq MHz (typ)	Clock to Output Delay ns (typ)	Power Dissipation mW (typ)	LSTTL Data Sheet Page No.
Parallel-in / Parallel-out Shift Right	74LS95	4	D	4S	⌝⌞	36	20	65	5-15
Parallel-in / Parallel-out Shift Right	74LS195	4	J, K	4S	⌟⌜	39	17	70	5-85
Parallel-in / Parallel-out Shift Right	74LS295	4	D	4S	⌟⌜	28	40	75	5-117
Parallel-in / Parallel-out Bi-Directional	74LS194	4	DR, DL	4S	⌟⌜	36	16	75	5-81
Serial-in / Parallel-out	74LS164	8	2D	-	⌟⌜	18	50	95	5-49
Parallel-in / Parallel-out	74LS174	6	-	6S	⌟⌜	40	21	65	5-57
Parallel-in / Parallel-out	74LS175	4	-	4S	⌟⌜	40	21	45	5-60
Parallel-in / Parallel-out	74LS298	4	-	2D MUX	⌝⌞	30	21	65	5-121
Multiport Registers	74LS170	16	-	4A	⌝⌞	-	25	125	5-53
Multiport Registers	74LS670	16	-	4A	⌝⌞	-	30	150	5-124

LOW POWER SCHOTTKY

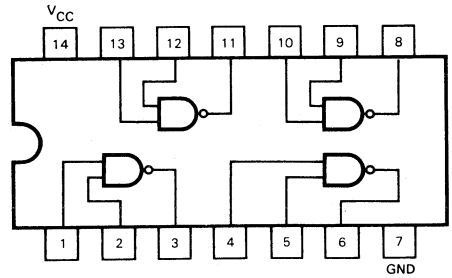


SSI Data Sheets

4

4

QUAD 2-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS00X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS00X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

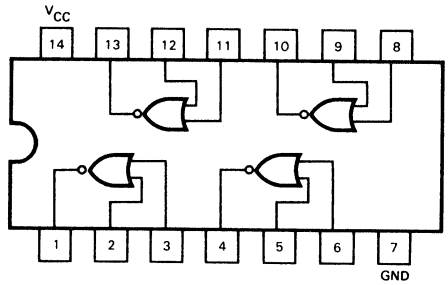
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS02X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS02X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

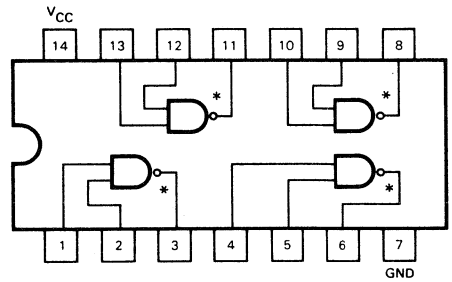
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.6	3.2	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	5.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS03X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS03X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

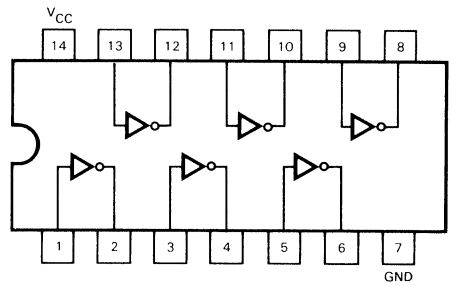
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

HEX INVERTER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS04X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS04X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

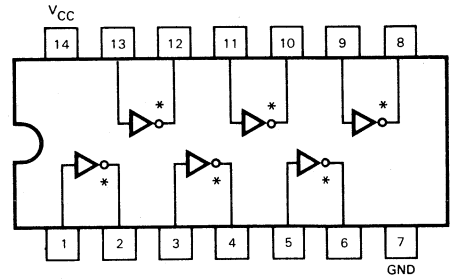
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.6	6.6	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

HEX INVERTER



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS05X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS05X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

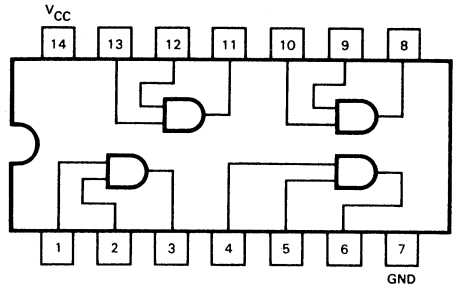
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.6	6.6	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

QUAD 2-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS08X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS08X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

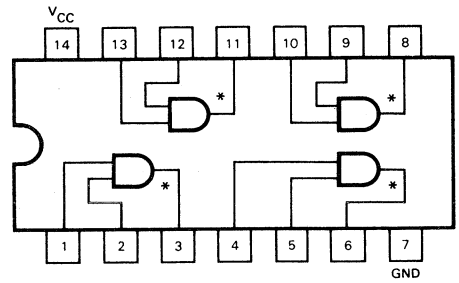
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			2.4	4.8	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.4	8.8	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		7.5	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT AND GATE (WITH OPEN-COLLECTOR OUTPUT)



*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS09X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS09X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

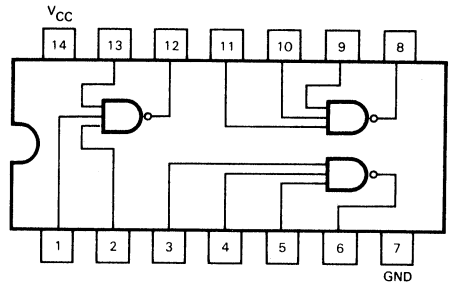
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			2.4	4.8	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.4	8.8	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		13	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

TRIPLE 3-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS10X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS10X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

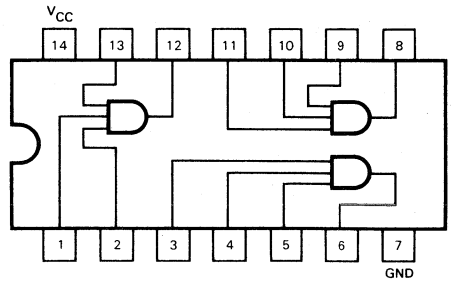
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.6	1.2	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.8	3.3	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	6.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	6.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

TRIPLE 3-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS11X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS11X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.8	3.6	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			3.3	6.6	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	4.0	8.5	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.5	11	ns	C_L = 15 pF

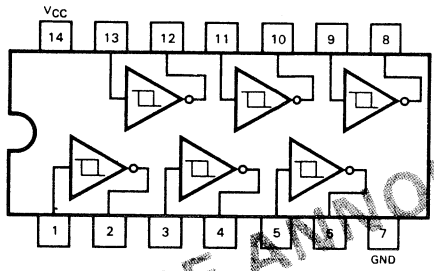
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

HEX SCHMITT TRIGGER INVERTER

DESCRIPTION – The SN54LS14/SN74LS14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{IN} VERSUS V_{OUT}
TRANSFER FUNCTION

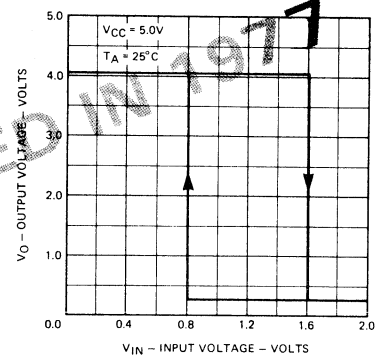


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
POWER SUPPLY VOLTAGE

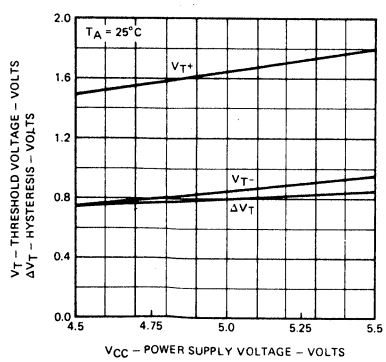


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS
VERSUS
TEMPERATURE

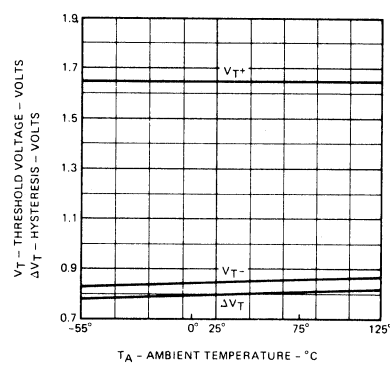


Fig. 3

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS14X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS14X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

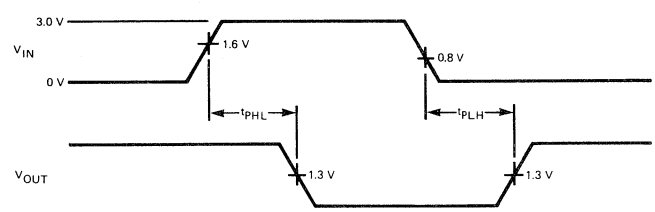
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{T+}	Positive-Going Threshold Voltage			1.6		V	V_{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage			0.8		V	V_{CC} = 5.0 V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			8.6	16	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			12	21	mA	V_{CC} = MAX, V_{IN} = 4.5 V

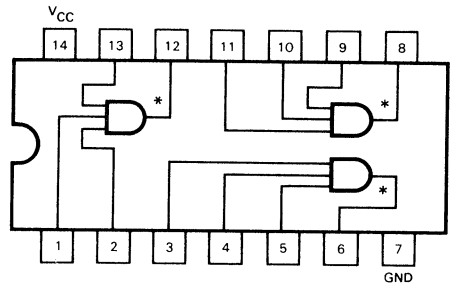
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Input to Output			20	ns	V_{CC} = 5.0 V
t_{PHL}	Propagation Delay, Input to Output			20	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



TRIPLE 3-INPUT AND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS15X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS15X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

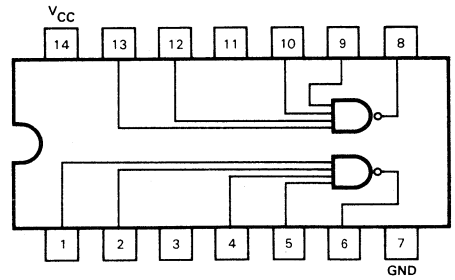
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			1.8	3.6	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			3.3	6.6	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	7.0	13	20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	5.0	10	15	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

DUAL 4-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS20X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS20X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

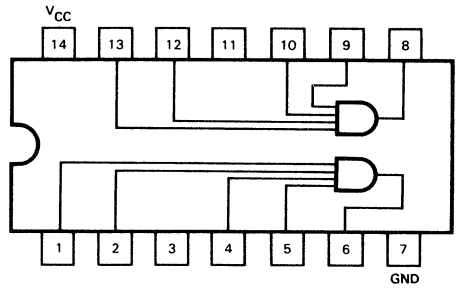
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.2	2.2	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	7.0	12	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.0	12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

DUAL 4-INPUT AND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS21X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS21X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

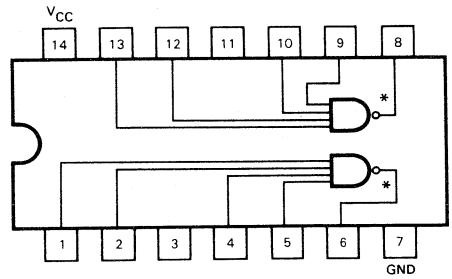
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			2.2	4.4	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

DUAL 4-INPUT NAND GATE



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS22X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS22X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

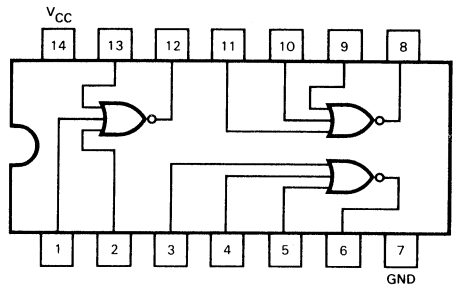
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.2	2.2	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

TRIPLE 3-INPUT NOR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS27X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS27X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

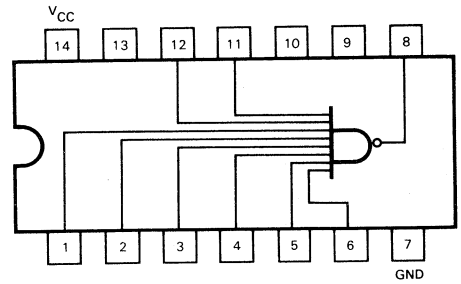
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			2.0	4.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.4	6.8	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

8-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS30X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS30X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

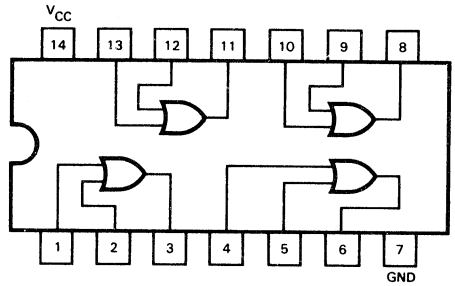
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.35	0.5	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.6	1.1	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		7.0	12	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		13	20	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT OR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS32X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS32X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

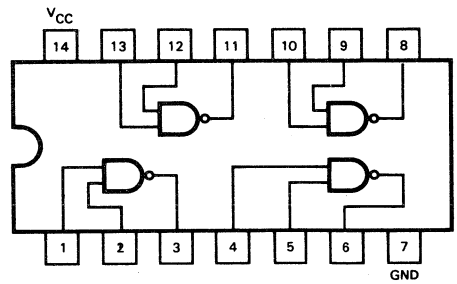
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			3.1	6.2	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.9	9.8	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	7.0	11	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.0	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS37X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS37X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

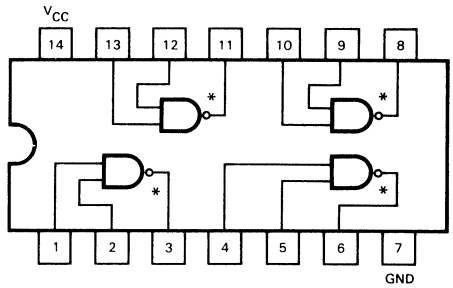
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −1.2 mA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.9	2.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			6.0	12	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 45 pF, R_L = 667 Ω

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT NAND BUFFER



*OPEN COLLECTOR OUTPUTS

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS38X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS38X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

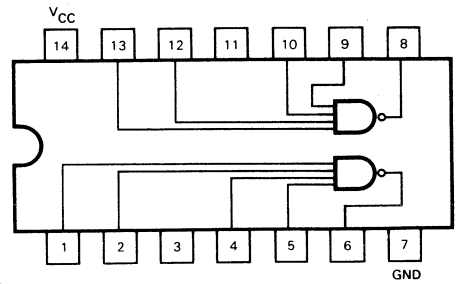
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				250	μA	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IN} = V_{IL}
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CCH}	Supply Current HIGH			0.9	2.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			6.0	12	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	18	ns	C_L = 45 pF, R_L = 667 Ω

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

DUAL 4-INPUT NAND BUFFER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS40X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS40X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

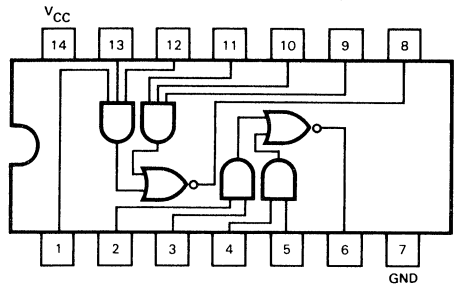
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −1.2 mA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 12 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 24 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.45	1.0	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.0	6.0	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 45 pF, R_L = 667 Ω

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS51X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS51X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

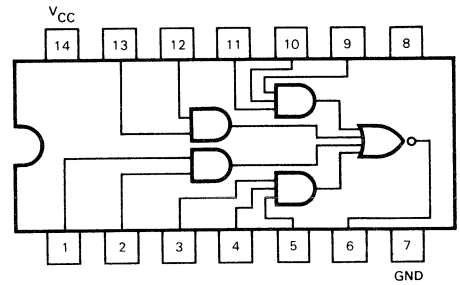
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.4	2.8	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		8.0	13	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		8.0	13	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

3-2-2-3-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS54X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS54X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

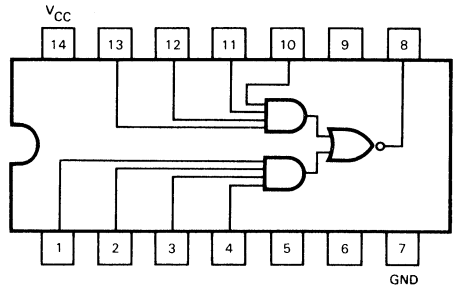
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			1.0	2.0	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

2-WIDE 4-INPUT AND-OR-INVERT GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS55X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS55X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.4	0.8	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.7	1.3	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

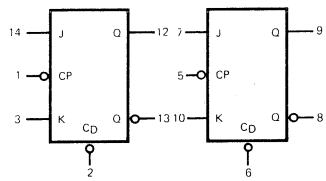
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		10	15	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

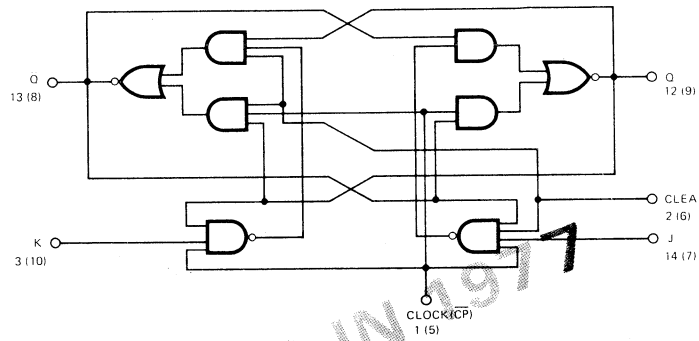
DESCRIPTION — The SN54LS73/SN74LS73 offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 4
GND = Pin 11

LOGIC DIAGRAM
(Each Flip-Flop)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS73X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS73X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current J, K Clear Clock				20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Clear Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Clear Clock				−0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: T_A = 25°C (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Clear to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K TO Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

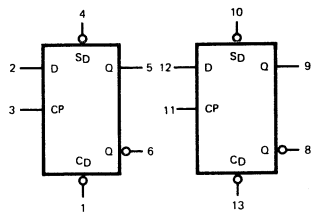
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION – The SN54LS74/SN74LS74 dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and $\overline{Q}$ outputs.

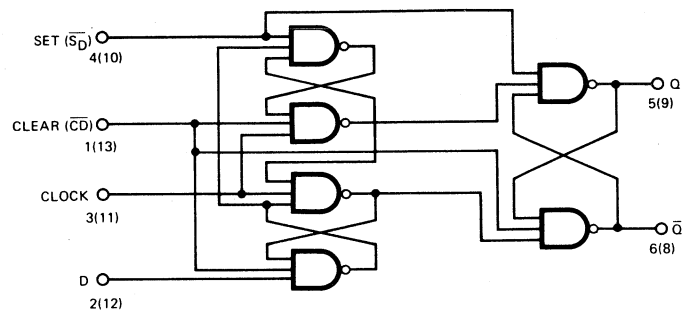
Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS74X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS74X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current Data Clock, Set Clear				20 40 60	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Data Clock, Set Clear				0.1 0.2 0.3	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current Data Clock, Set Clear				−0.4 −0.8 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

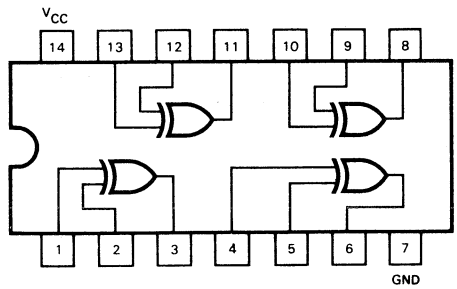
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency		30	45		MHz	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			15 22	20 30	ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH}	Propagation Delay,			10	15	ns	Fig. 2	
t_{PHL}	Set or Clear to Output	CP = L		18	24			
t_{PHL}		CP = H		26	35			

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_wCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 1	
t_w	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, Data to Clock	10	6		ns	Fig. 1	V_{CC} = 5.0 V
t_h(H)	Hold Time HIGH, Data to Clock	0	−14		ns		
t_s(L)	Set-up Time LOW, Data to Clock	20	14		ns		
t_h(L)	Hold Time LOW, Data to Clock	0	−6		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

QUAD 2-INPUT EXCLUSIVE OR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS86X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN54LS86X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5	V	I_{OL} = 8.0 mA or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 5)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current			6.1	10	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

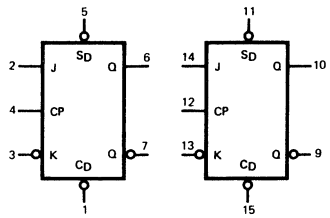
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			12 17	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			10 12	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

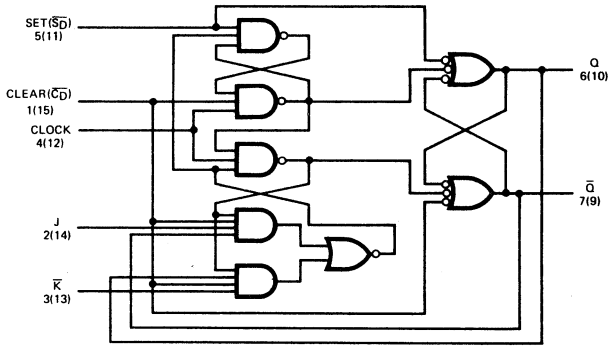
DESCRIPTION — The SN54LS109/SN74LS109 consists of two high speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS109X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS109X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current J, K Clock, Set Clear				20 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Clock, Set Clear				0.1 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Clock, Set Clear				−0.4 −0.8 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency		30	45		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			15 22	20 30	ns	Fig. 1	
t_{PLH} t_{PHL} t_{PHL}	Propagation Delay, Set or Clear to Output	CP = L CP = H		10 18 26	15 24 35	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

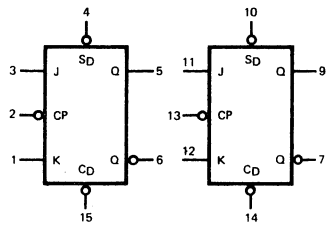
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 1	V_{CC} = 5.0 V
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, Data to Clock	18	12		ns	Fig. 1	
t_h(H)	Hold Time HIGH, Data to Clock	0	−13		ns		
t_s(L)	Set-up Time LOW, Data to Clock	20	13		ns		
t_h(L)	Hold Time LOW, Data to Clock	0	−12		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

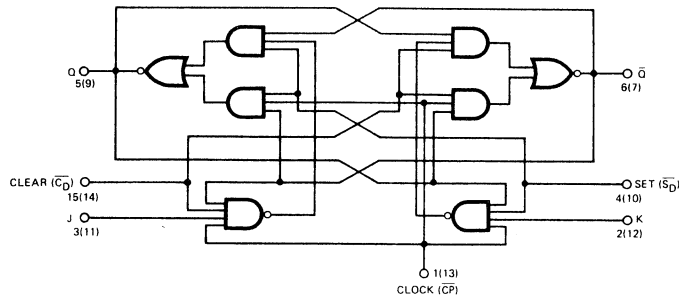
DESCRIPTION — The SN54LS112/SN74LS112 dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS112X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS112X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set, Clear Clock				 20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	 J, K Set, Clear Clock				 0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set, Clear Clock				 −0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: T_A = 25°C (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C (See Page 4-51 for Waveforms)

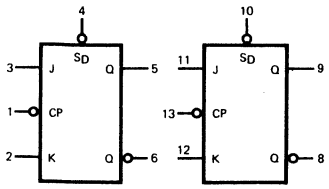
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K to Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

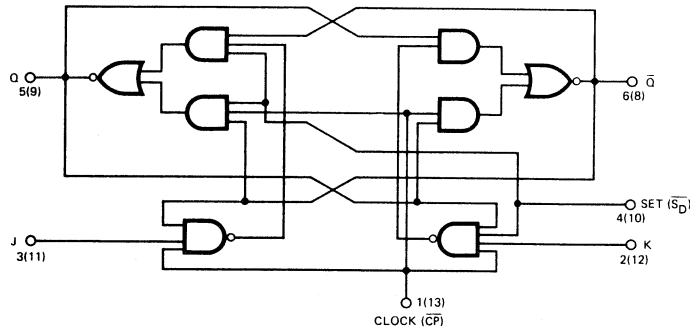
DESCRIPTION — The SN54LS113/SN74LS113 offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS113X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS113X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set Clock				20 60 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set Clock				0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set Clock				−0.36 −0.8 −0.72	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	J	K	Q	$\overline{Q}$
Set	L	X	X	H	L
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set to Output		11 16	16 24	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

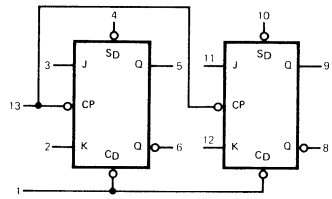
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K to Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

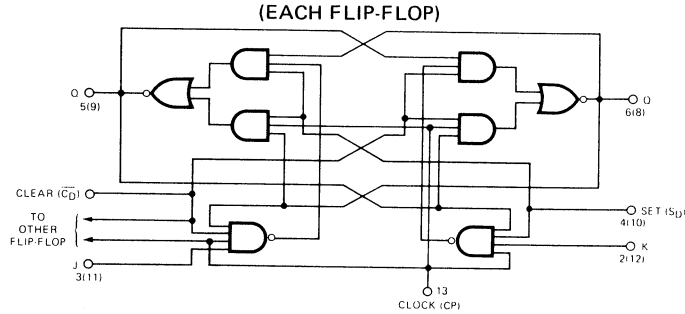
DESCRIPTION — The SN54LS114/SN74LS114 offers common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC DIAGRAM
(EACH FLIP-FLOP)



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS114X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS114X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current J, K Set Clear Clock				20 60 120 160	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	J, K Set Clear Clock				0.1 0.3 0.6 0.8	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current J, K Set Clear Clock				−0.36 −0.8 −1.6 −1.44	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.0	8.0	mA	V_{CC} = MAX, V_{CP} = 0 V

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

*Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

AC CHARACTERISTICS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

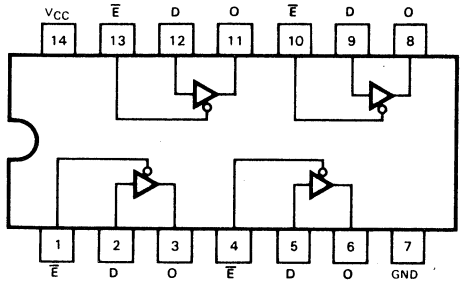
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Clock Frequency	30	45		MHz	Fig. 3	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		11 16	16 24	ns	Fig. 3	
t_{PLH} t_{PHL}	Propagation Delay, Set or Clear to Output		11 16	16 24	ns	Fig. 2	

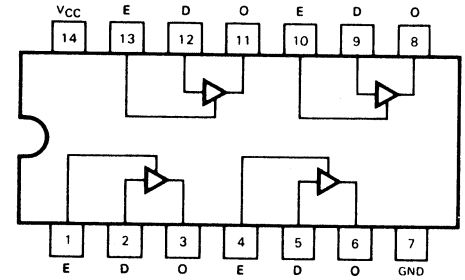
AC SET-UP REQUIREMENTS: $T_A = 25°C$ (See Page 4-51 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_WCP(H)	Clock Pulse Width (HIGH)	18	12		ns	Fig. 3	V_{CC} = 5.0 V
t_WCP(L)	Clock Pulse Width (LOW)	15	10		ns		
t_W	Set or Clear Pulse Width	15	10		ns	Fig. 2	
t_s(H)	Set-up Time HIGH, J or K to Clock	20	13		ns	Fig. 3	
t_h(H)	Hold Time HIGH, J or K to Clock	0	−10		ns		
t_s(L)	Set-up Time LOW, J or K to Clock	15	10		ns		
t_h(L)	Hold Time LOW, J or K to Clock	0	−13		ns		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
5. HOLD TIME (t_h) is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

QUAD 3-STATE BUFFERS WITH ACTIVE HIGH ENABLES





GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS125X SN54LS126X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS125X SN74LS126X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = V_{IL}
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = V_{IL}
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs LOW	LS125			16	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V
		LS126			20	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V
	Power Supply Current, Outputs Off	LS125			20	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V
		LS126			24	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 0 V

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

TRUTH TABLES

LS125

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

LS126

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
(Z) = High Impedance (off)

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			10 16	ns	Fig. 2	V_{CC} = 5.0 V C_L = 45 pF R_L = 667 Ω
t_{PZH}	Output Enable Time to HIGH Level			16	ns	Figs. 4, 5	
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level			15	ns	Figs. 3, 5	V_{CC} = 5.0 V C_L = 5 pF R_L = 667 Ω
t_{PHZ}	Output Disable Time from HIGH Level			23	ns	Figs. 4, 5	

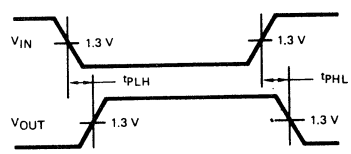


Fig. 1

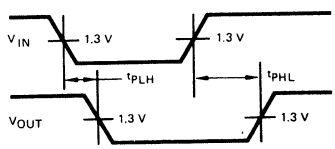


Fig. 2

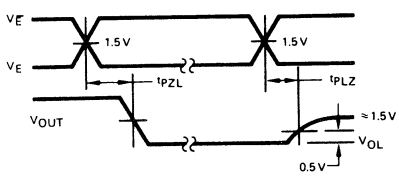


Fig. 3

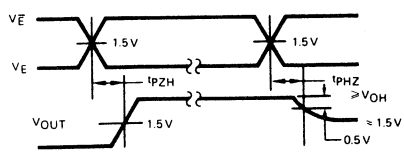
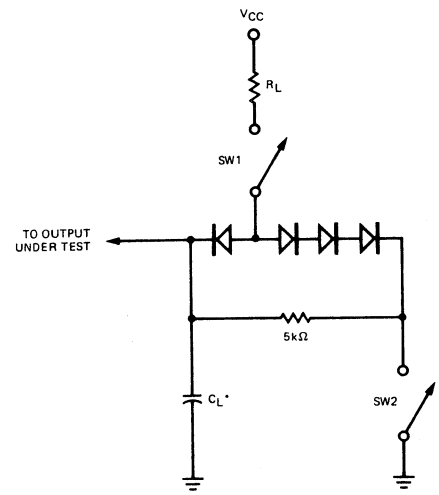


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

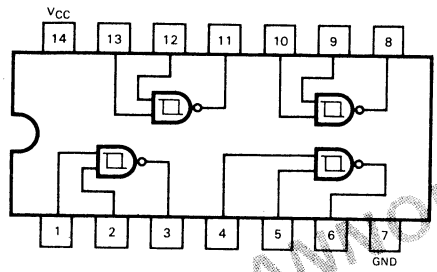
Fig. 5

QUAD 2-INPUT SCHMITT TRIGGER NAND GATE

DESCRIPTION – The SN54LS132/SN74LS132 contains four 2-Input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+} (MAX), the gate will respond to the transitions of the other input as shown in Figure 1.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{IN} VERSUS V_{OUT} TRANSFER FUNCTION

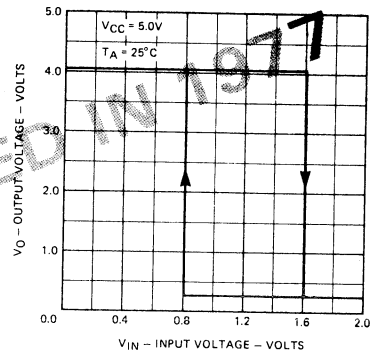


Fig. 1

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS POWER SUPPLY VOLTAGE

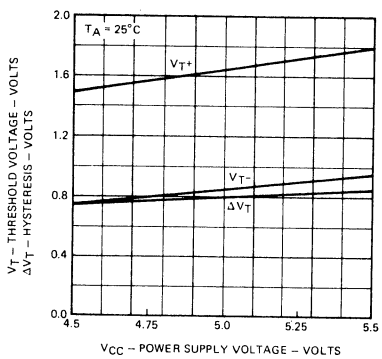


Fig. 2

THRESHOLD VOLTAGE AND HYSTERESIS VERSUS TEMPERATURE

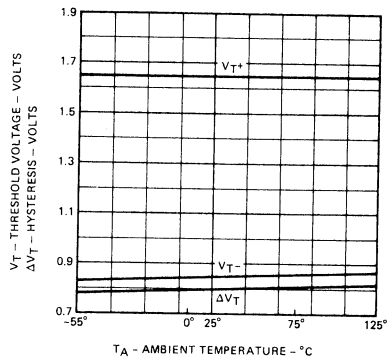


Fig. 3

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS132X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS132X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

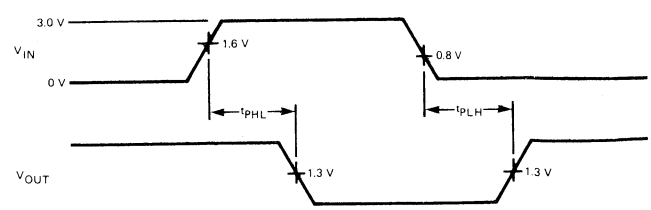
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{T+}	Positive-Going Threshold Voltage			1.6		V	V_{CC} = 5.0 V
V_{T-}	Negative-Going Threshold Voltage			0.8		V	V_{CC} = 5.0 V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{T+}	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			5.9	11	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			8.2	14	mA	V_{CC} = MAX, V_{IN} = 4.5 V

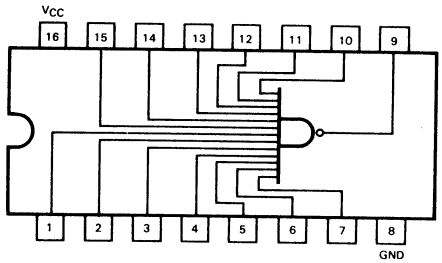
AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output			20	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output			20	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



13-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS133X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS133X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

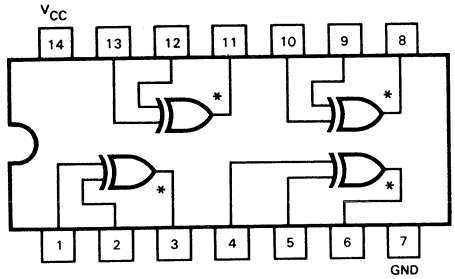
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.35	0.5	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			0.6	1.1	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		20	30	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

QUAD 2-INPUT EXCLUSIVE OR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS136X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS136X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

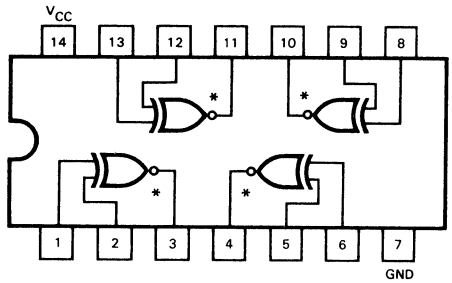
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V; V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current			6.1	10	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			23 23	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			23 23	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

QUAD 2-INPUT EXCLUSIVE NOR GATE



TRUTH TABLE

IN		OUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

*Open Collector Outputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS266X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS266X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

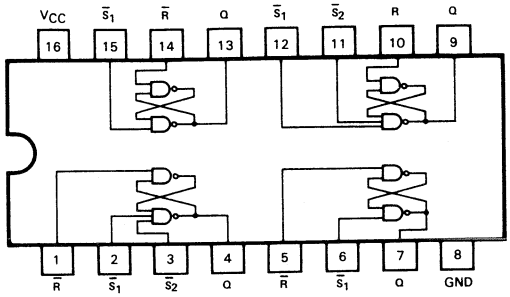
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V; V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{CC}	Power Supply Current			8.0	13	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW			23 23	ns	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH			23 23	ns	C_L = 15 pF, R_L = 2.0 kΩ

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.

QUAD SET-RESET LATCH



TRUTH TABLE

INPUTS			OUTPUT
$\bar{S}_1$	$\bar{S}_2$	$\bar{R}$	(Q)
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS279X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS279X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

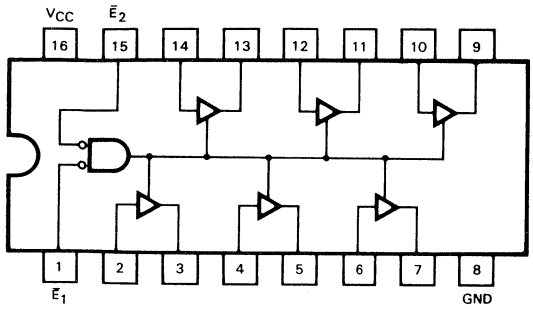
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			3.8	7.0	mA	V_{CC} = MAX

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (See Page 4-50 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, $\bar{S}$ to Output			22 15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Propagation Delay, $\bar{R}$ to Output			27	ns	

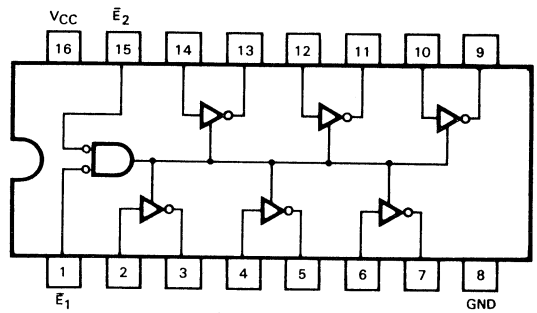
SN54LS365/SN74LS365
HEX 3-STATE BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

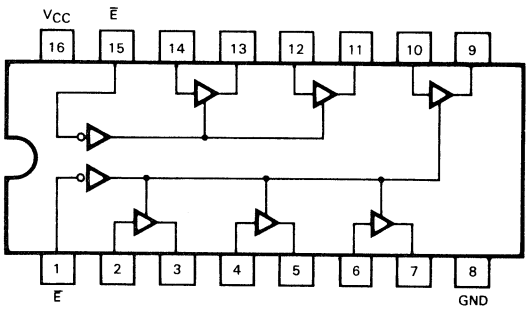
SN54LS366/SN74LS366
HEX 3-STATE INVERTER BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

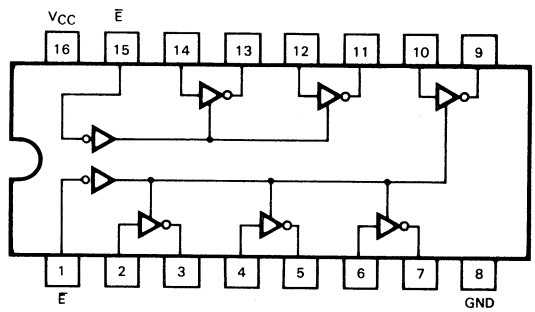
SN54LS367/SN74LS367
HEX 3-STATE BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

SN54LS368/SN74LS368
HEX 3-STATE INVERTER BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	H
L	H	L
H	X	(Z)

DESCRIPTION — The LS365/366/367/368 are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable ($\overline{E}$) is LOW.

When the Output Enable Input ($\overline{E}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

GUARANTEED OPERATING RANGES

PART NUMBERS		SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
SN54LS365X SN54LS367X	SN54LS366X SN54LS368X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS365X SN74LS367X	SN74LS366X SN74LS368X	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4			I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	LS365/367		13.5	24	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	
		LS366/368		11.8	21			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 4-41 for Waveforms)

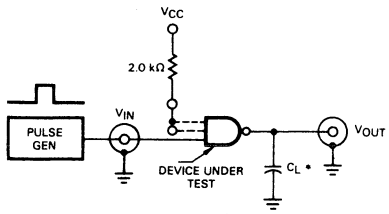
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output (LS365 • LS367)			10 16	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output (LS366 • LS368)			10 16	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			16	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			15	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			23	ns	Figs. 4, 5	R_L = 667 Ω

AC WAVEFORMS

AC TEST CIRCUITS AND WAVEFORMS

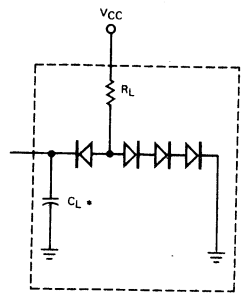
The following test circuits and conditions represent Motorola's typical AC test procedures. The output loading for standard Low Power Schottky devices is a 15 pF capacitor. Experimental evidence shows that test results using the additional diode-resistor load are within 0.2 ns of the capacitor only load. The capacitor only load also has the advantage of repeatable, easily correlated test results. The input pulse rise and fall times are specified at 6 ns to closely approximate the Low Power Schottky output transitions through the active threshold region. The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15 MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

Test Circuit for Standard Output Devices

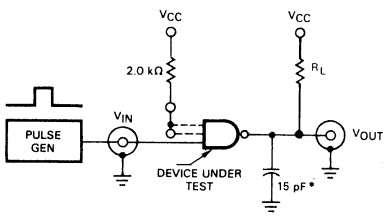


*Includes all probe and jig capacitance

Optional Load (Guaranteed—Not Tested)



Test Circuit for Open Collector Output Devices

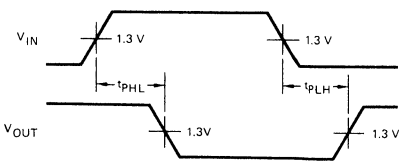


*Includes all probe and jig capacitance

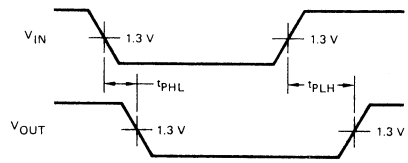
Pulse Generator Settings
(unless otherwise specified)

Frequency = 1 mHz
Duty Cycle = 50%
t_{TLH} (t_r) = 6 ns
t_{THL} (t_f) = 6 ns
Amplitude = 0 to 3 V

Waveform for Inverting Outputs



Waveform for Non-inverting Outputs



AC WAVEFORMS

WAVEFORMS FOR LS73, LS74, LS109, LS112, LS113, AND LS114

Fig. 1 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH

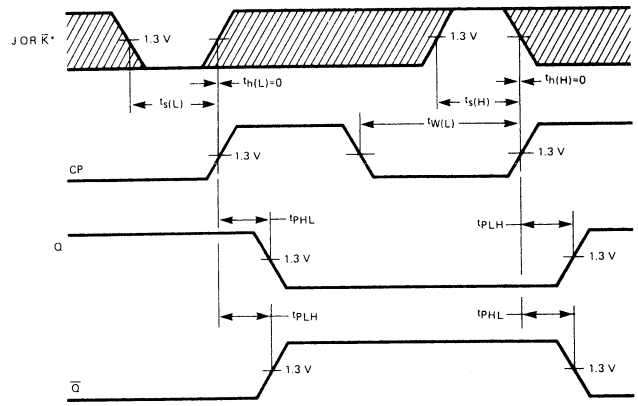


Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS

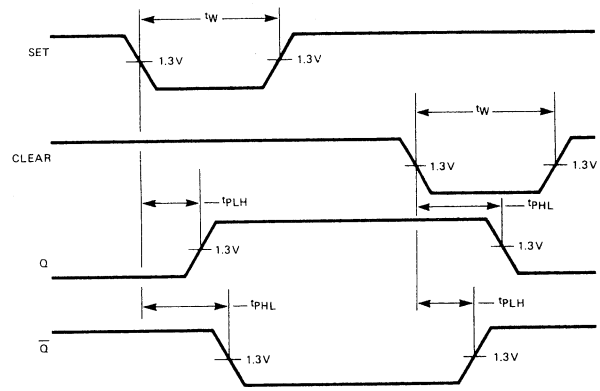
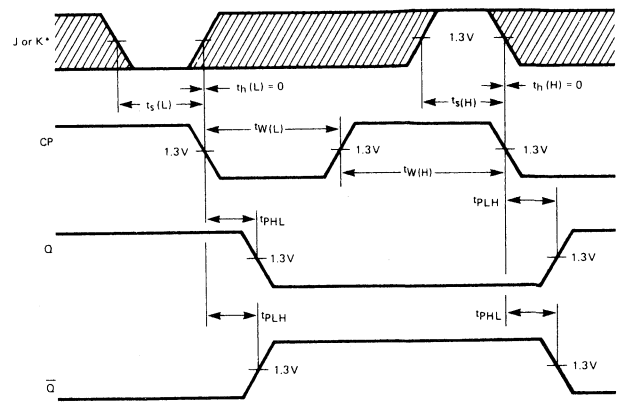
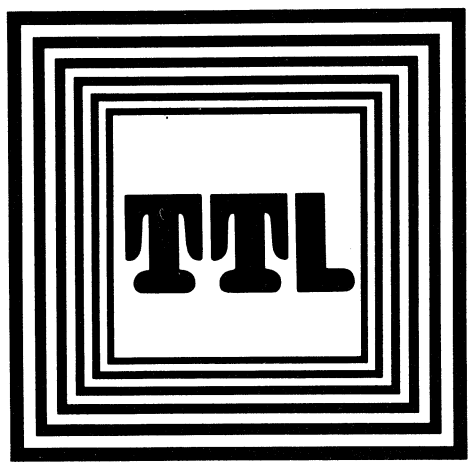


Fig. 3 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH



*The shaded areas indicate when the input is permitted to change for predicatable output performance.

LOW POWER SCHOTTKY



MSI Data Sheets 5

5

SN54LS42/SN74LS42

ONE-OF-TEN DECODER

DESCRIPTION — The LSTTL/MSI SN54LS42/SN74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

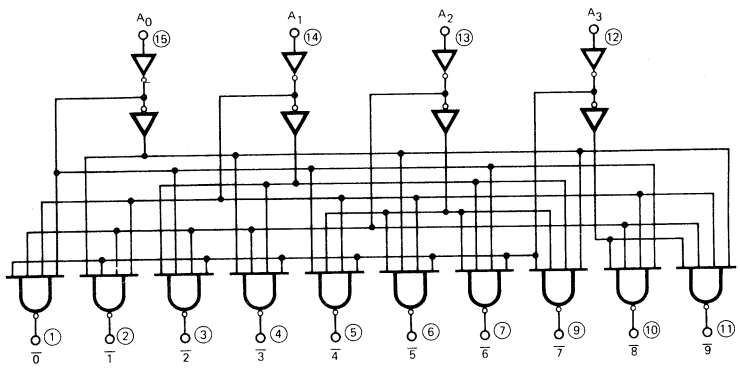
- MULTI-FUNCTION CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- DEMULTIPLEXING CAPABILITY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$A_0 - A_3$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.	5(2.5) U.L.

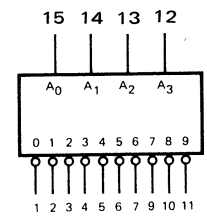
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



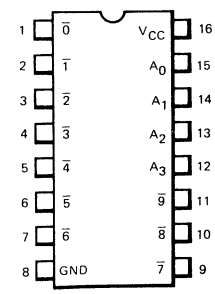
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the LS42 is used as a one-of-eight decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS42X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS42X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			7.0	12	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay (2 Levels)		11 18	18 25	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay (3 Levels)		12 19	20 27	ns	Fig. 1	

AC WAVEFORMS

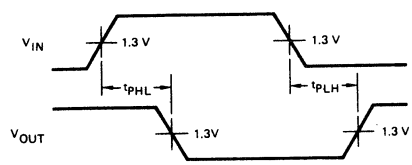


Fig. 1

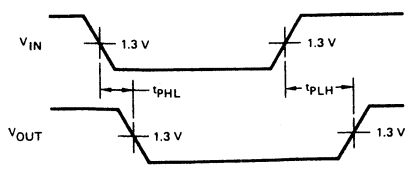


Fig. 2

SN54LS83A/SN74LS83A

4-BIT BINARY FULL ADDER WITH FAST CARRY

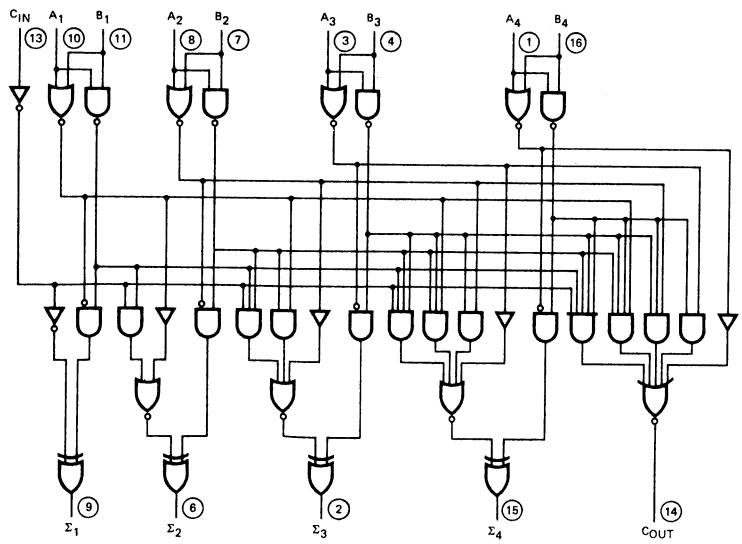
DESCRIPTION — The SN54LS83A/SN74LS83A is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ($A_1 - A_4$, $B_1 - B_4$) and a Carry Input (C_{IN}). It generates the binary Sum outputs ($\Sigma_1 - \Sigma_4$) and the Carry Output (C_{OUT}) from the most significant bit. The LS83 operates with either active HIGH or active LOW operands (positive or negative logic). The SN54LS283/SN74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_{IN}	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_{OUT}	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

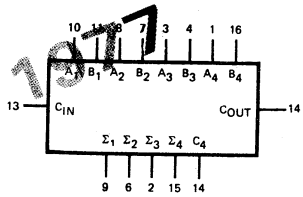
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



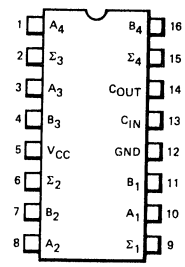
V_{CC} = Pin 5
GND = Pin 12
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS83 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_{OUT}) outputs.

$$C_{IN}+(A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_{OUT}$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1, can be arbitrarily assigned to pins 10, 11, 13, etc.

ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS83AX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS83AX	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current C_{IN} Any A or B				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	C_{IN} Any A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current C_{IN} Any A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			22	39	mA	V_{CC} = MAX, All Inputs 0 V
				19	34	mA	V_{CC} = MAX, A Inputs = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output			24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs			24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to C_{OUT} Output			17 17	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_{OUT} Output			17 17	ns	

AC WAVEFORMS

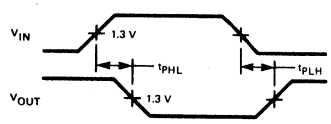


Fig. 1

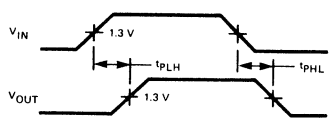


Fig. 2

SN54LS90/SN74LS90 • SN54LS92/SN74LS92

DECADE COUNTER DIVIDE-BY-TWELVE COUNTER

SN54LS93/SN74LS93

4-BIT BINARY COUNTER

DESCRIPTION – The SN54LS90/SN74LS90, SN54LS92/SN74LS92 and SN54LS93/SN74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- **LOW POWER CONSUMPTION . . . TYPICALLY 45 mW**
- **HIGH COUNT RATES . . . TYPICALLY 50 MHz**
- **CHOICE OF COUNTING MODES . . . BCD, BI-QUINARY, DIVIDE-BY-TWELVE, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	3.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS90), ÷6 Section (LS92)	2.0 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS93)	1.0 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (LS90), ÷6 (LS92), ÷8 (LS93) Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:

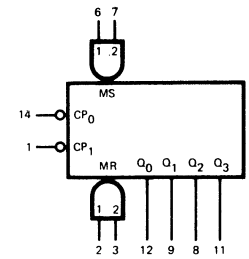
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.

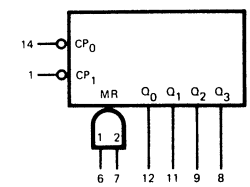
LOGIC SYMBOL

LS90



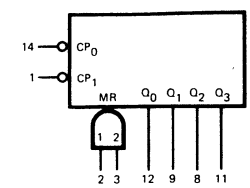
V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 13

LS92



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 2, 3, 4, 13

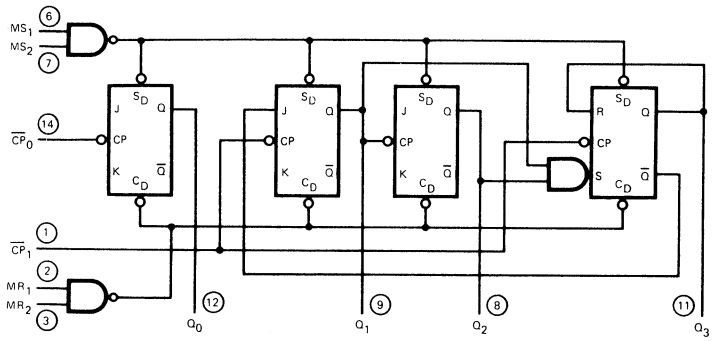
LS93



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

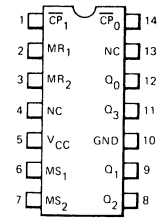
LOGIC DIAGRAM

LS90



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

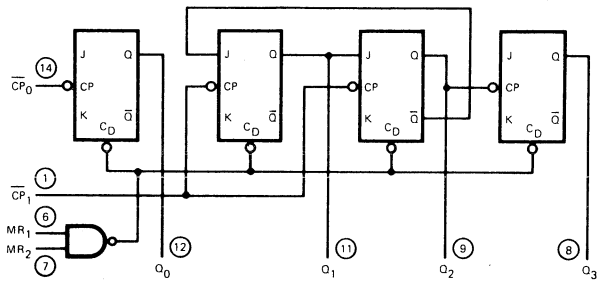


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

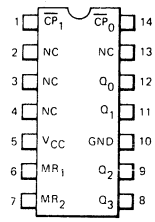
LOGIC DIAGRAM

LS92



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

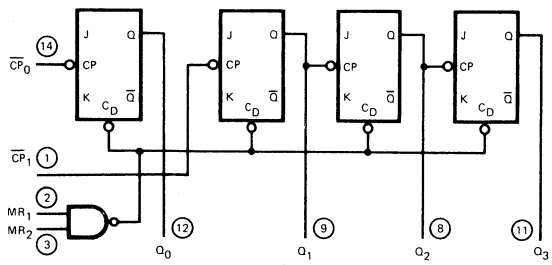


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

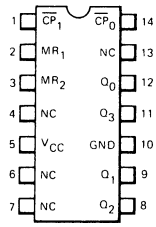
LOGIC DIAGRAM

LS93



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \bullet MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \bullet MS_2$) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.:

LS90

A. BCD Decade (8421) Counter – The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter – The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter – No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

A. Modulo 12, Divide-By-Twelve Counter – The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter – No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

LS93

A. 4-Bit Ripple Counter – The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter – The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS90
MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS92 AND LS93
MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS90
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

LS92
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Note: Output Q_0 connected to input CP_1.

LS93
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS90X SN54LS92X SN54LS93X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS90X SN74LS92X SN74LS93X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS93) $\overline{CP}_1$ (LS90, LS92)				20 120 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	MS, MR $\overline{CP}_0$, $\overline{CP}_1$ (LS93) $\overline{CP}_1$ (LS90, LS92)				0.1 0.4 0.8	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS93) $\overline{CP}_1$ (LS90, LS92)				−0.4 −2.4 −1.6 −3.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9	15	mA	V_{CC} = MAX

NOTES

1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF

SYMBOL	PARAMETER	LIMITS						UNITS	
		LS90		LS92		LS93			
		MIN	MAX	MIN	MAX	MIN	MAX		
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		32		MHz	Fig. 1
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		16		MHz	Fig. 1
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18		16 18	ns	Fig. 1
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		16 21		16 21		16 21	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		32 35		16 21		32 35	ns	
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		32 35		32 35		51 51	ns	
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_3 Output		48 50		48 50		70 70	ns	
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30					ns	Fig. 3
t_{PHL}	MS Input to Q_1 and Q_2Outputs		40					ns	Fig. 2
t_{PHL}	MR Input to Any Output		40		40		40	ns	Fig. 2

AC SET-UP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

SYMBOL	PARAMETER	LIMITS						UNITS	
		LS90		LS92		LS93			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_W	$\overline{CP}_0$ Pulse Width	15		15		15		ns	Fig. 1
t_W	$\overline{CP}_1$ Pulse Width	30		30		30		ns	
t_W	MS Pulse Width	15						ns	Fig. 2, 3
t_W	MR Pulse Width	15		15		15		ns	Fig. 2
t_{rec}	Recovery Time MS to $\overline{CP}$	25						ns	Fig. 2, 3
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		ns	Fig. 2

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

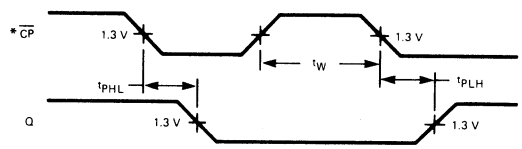


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

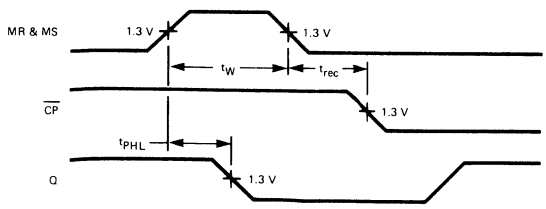


Fig. 2

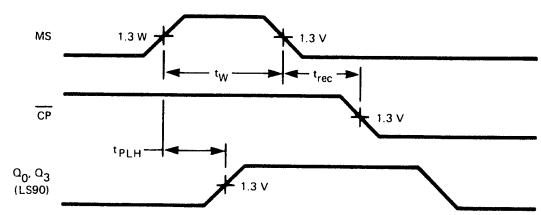


Fig. 3

SN54LS95B/SN74LS95B

4-BIT SHIFT REGISTER

DESCRIPTION — The SN54LS95B/SN74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

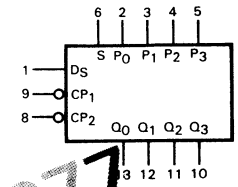
- **SYNCHRONOUS, EXPANDABLE SHIFT RIGHT**
- **SYNCHRONOUS SHIFT LEFT CAPABILITY**
- **SYNCHRONOUS PARALLEL LOAD**
- **SEPARATE SHIFT AND LOAD CLOCK INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Mode Control Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{CP}_1$	Serial Clock (Active LOW Going Edge) Input	1.0 U.L.	0.5 U.L.
$\overline{CP}_2$	Parallel Clock (Active LOW Going Edge) Input	1.0 U.L.	0.5 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

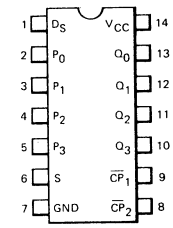
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



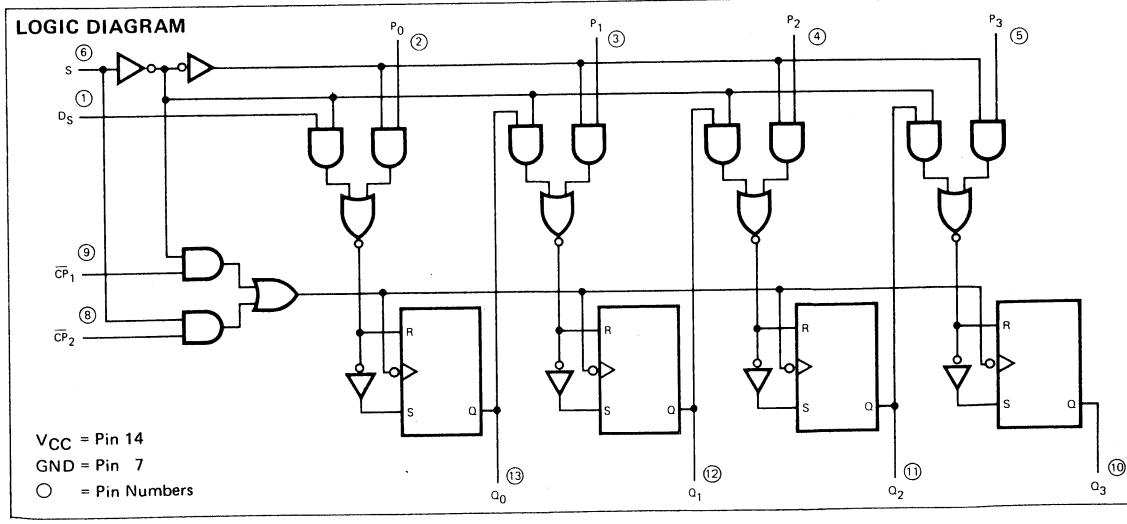
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The LS95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel ($P_0 - P_3$) Data inputs and four Parallel Data outputs ($Q_0 - Q_3$). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock inputs ($\overline{CP}_1$) and ($\overline{CP}_2$). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_2$ transfers parallel data from the $P_0 - P_3$ inputs to the $Q_0 - Q_3$ outputs.

When the Mode Control input (S) is LOW, $\overline{CP}_1$ is enabled. A HIGH to LOW transition on enabled $\overline{CP}_1$ transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1, and Q_1 to P_0, and operating the 9LS95 in the parallel mode (S = HIGH).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while $\overline{CP}_2$ is HIGH, or changing S from HIGH to LOW while $\overline{CP}_1$ is HIGH and $\overline{CP}_2$ is LOW will not cause any changes on the register outputs.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	$\overline{CP}_1$	$\overline{CP}_2$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	↓	X	l	X	L	q_0	q_1	q_2
	L	↓	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	↓	X	P_n	p_0	p_1	p_2	p_3
Mode Change	↓	L	L	X	X	No Change			
	↑	L	L	X	X	No Change			
	↓	H	L	X	X	No Change			
	↑	H	L	X	X	Undetermined			
	↓	L	H	X	X	Undetermined			
	↑	L	H	X	X	No Change			
	↓	H	H	X	X	Undetermined			
	↑	H	H	X	X	No Change			

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.
p_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS95BX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS95BX	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current S, D_S, P_0, P_1, P_2, P_3				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{CP}_1$, $\overline{CP}_2$				40		
	S, D_S, P_0, P_1, P_2, P_3				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{CP}_1$, $\overline{CP}_2$				0.2		
I_{IL}	Input LOW Current S, D_S, P_0, P_1, P_2, P_3				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{CP}_1$, $\overline{CP}_2$				−0.8		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			13	21	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		20 18	27 27	ns	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_{W(CP)}$	Clock Pulse Width	20			ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
$t_{s(Data)}$	Set-up Time, Data to Clock	20			ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	10			ns	Fig. 1	
t_{sL}	Set-up Time, LOW Mode Control to Clock	20			ns	Fig. 2	
t_{hL}	Hold Time, LOW Mode Control to Clock	0			ns	Fig. 2	
t_{sH}	Set-up Time, HIGH Mode Control to Clock	20			ns	Fig. 2	
t_{hH}	Hold Time, HIGH Mode Control to Clock	0			ns	Fig. 2	

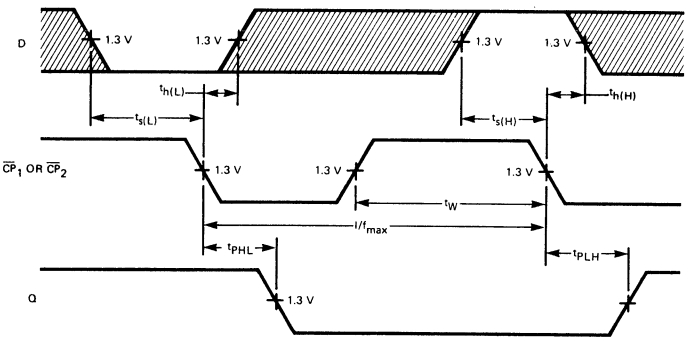
DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is (D_S for $\overline{CP}_1$) or (P_n for $\overline{CP}_2$).

Fig. 1

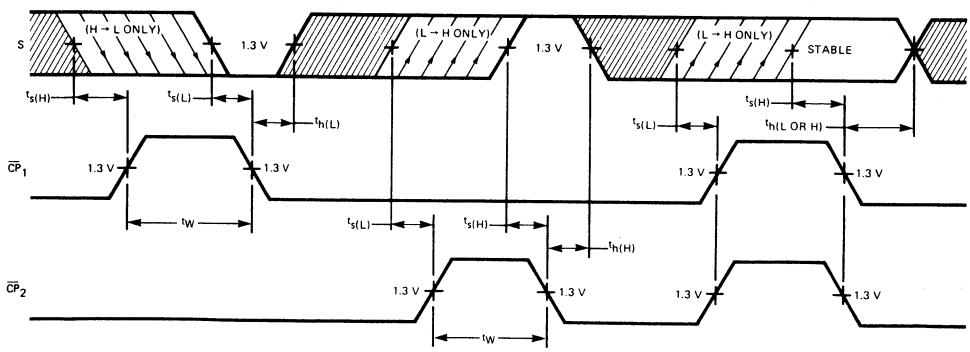


Fig. 2

SN54LS138/SN74LS138

1-OF-8 DECODER/DEMULTIPLEXER

DESCRIPTION – The LSTTL/MSI SN54LS138/SN74LS138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

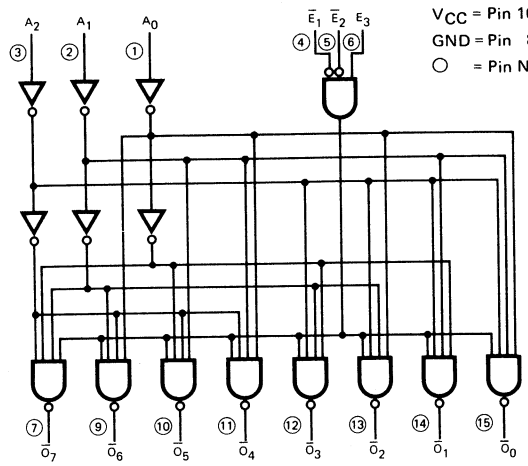
- **DEMULTIPLEXING CAPABILITY**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION**
- **TYPICAL POWER DISSIPATION OF 32 mW**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

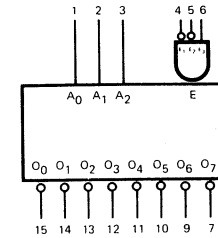
		LOADING (Note a) HIGH	LOW
$A_0 - A_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1, \overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_7$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

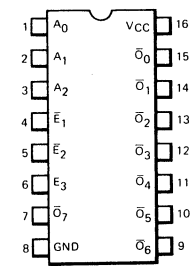


LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

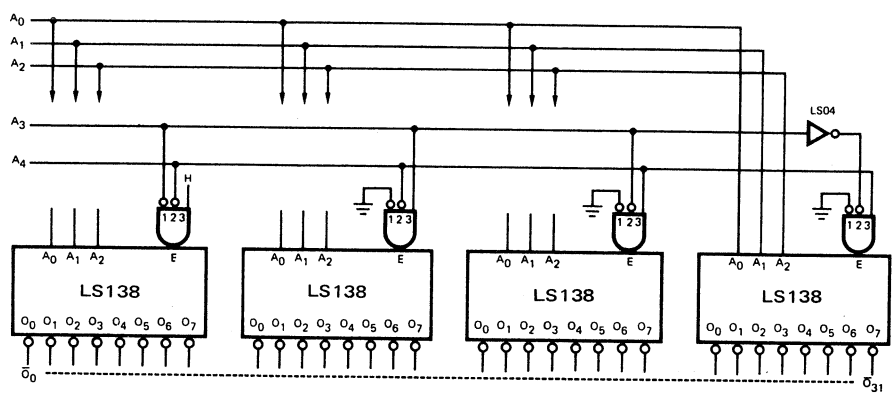


Fig. a.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS138X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS138X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.3	10	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Address to Output		11 19	18 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E_1}$ or $\overline{E_2}$ to Output		9.0 17	15 24	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, E_3 to Output		11 20	18 28	ns	Fig. 1	

AC WAVEFORMS

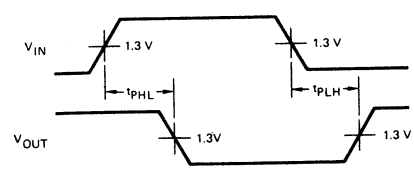


Fig. 1

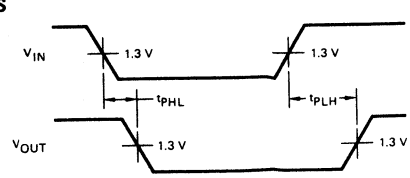


Fig. 2

SN54LS139/SN74LS139

DUAL 1-OF-4 DECODER

DESCRIPTION — The LSTTL/MSI SN54LS139/SN74LS139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

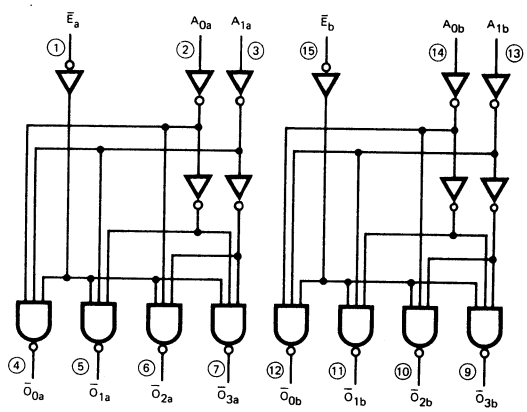
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **TWO COMPLETELY INDEPENDENT 1-OF-4 DECODERS**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

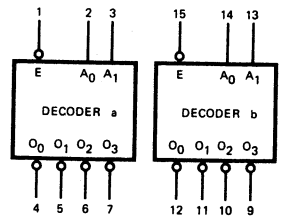
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



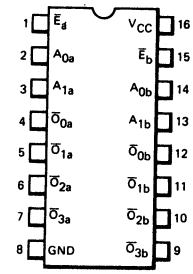
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

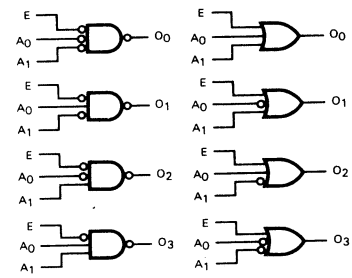


Fig. a

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS139X	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS139X	4.75 V	5.0 V	5.25 V	0°C to + 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.8	11	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		11 19	18 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		9.0 17	15 24	ns	Fig. 2	

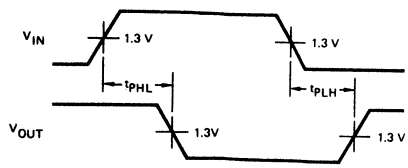


Fig. 1

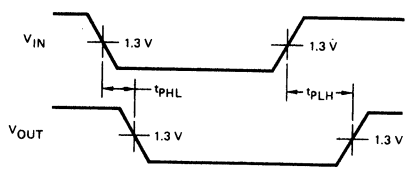


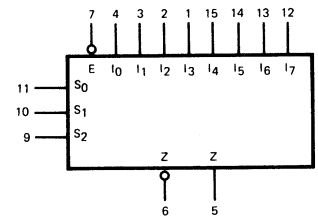
Fig. 2

SN54LS151/SN74LS151
8-INPUT MULTIPLEXER

DESCRIPTION — The TTL/MSI SN54LS151/SN74LS151 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

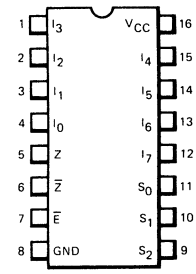
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



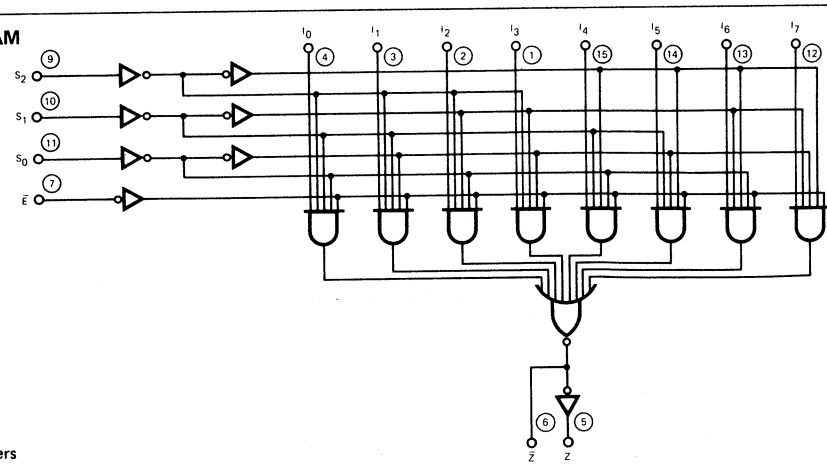
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS151 can provide any logic function of four variables and its negation.

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS151X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS151X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.0	10	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		11 23	20 32	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		30 18	41 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Z}$ Output		13 17	20 26	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Z Output		22 18	33 27	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		7.0 10	12 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		18 15	26 23	ns	Fig. 2	

AC WAVEFORMS

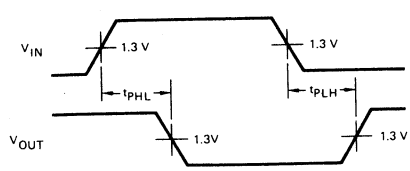


Fig. 1

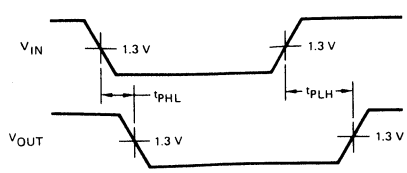


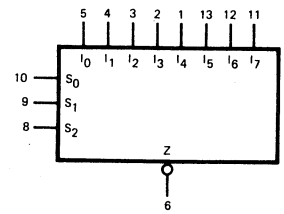
Fig. 2

SN54LS152/SN74LS152
8-INPUT MULTIPLEXER

DESCRIPTION — The TTL/MSI SN54LS152/SN74LS152 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS152 can be used as a universal function generator to generate any logic function of four variables. It is supplied in FLATPAK only; for Dual In-line Package application use the LS151.

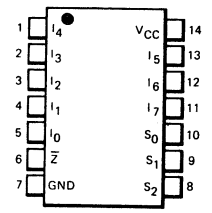
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
FLATPAK (TOP VIEW)



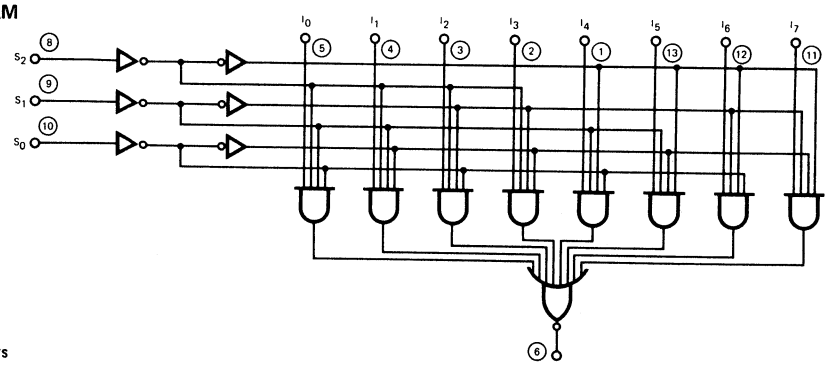
Dot Indicates Pin 1

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. The logic function provided at the output is:

$$\overline{Z} = (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The LS152 provides the ability, in one package, to select from eight sources of data or control information.

TRUTH TABLE

S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$
X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	X	X	X	X	X	X	X	H
L	L	L	H	X	X	X	X	X	X	X	L
L	L	H	X	L	X	X	X	X	X	X	H
L	L	H	X	H	X	X	X	X	X	X	L
L	H	L	X	X	L	X	X	X	X	X	H
L	H	L	X	X	H	X	X	X	X	X	L
L	H	H	X	X	X	L	X	X	X	X	H
L	H	H	X	X	X	H	X	X	X	X	L
H	L	L	X	X	X	X	L	X	X	X	H
H	L	L	X	X	X	X	H	X	X	X	L
H	L	H	X	X	X	X	X	L	X	X	H
H	L	H	X	X	X	X	X	H	X	X	L
H	H	L	X	X	X	X	X	X	L	X	H
H	H	L	X	X	X	X	X	X	H	X	L
H	H	H	X	X	X	X	X	X	X	L	H
H	H	H	X	X	X	X	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS152X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS152X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			5.6	9.0	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		12 23	20 32	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		8.0 10	13 15	ns	Fig. 1	

AC WAVEFORMS

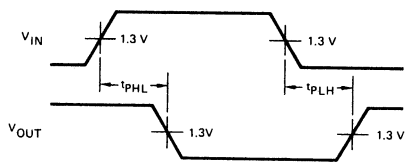


Fig. 1

SN54LS153/SN74LS153

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION – The LSTTL/MSI SN54LS153/SN74LS153 is a very high speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the LS153 can generate any two functions of three variables. The LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

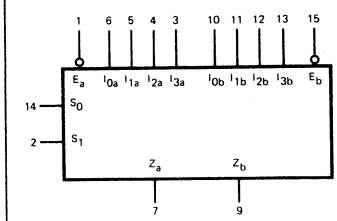
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING OUTPUTS**
- **SEPARATE ENABLE FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S_0	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	10 U.L.	5 (2.5) U.L.

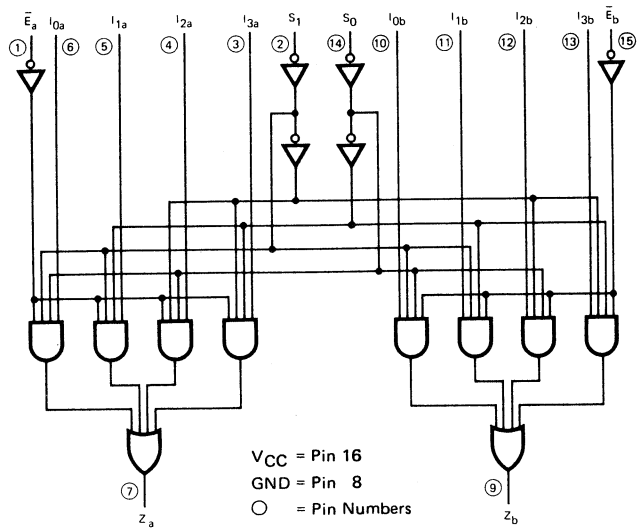
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

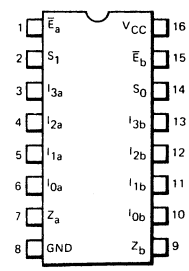


V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS153 is a Dual 4-Input Multiplexer fabricated with Low Power, Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW.

The LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS153X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS153X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.2	10	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output		20 16	29 24	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		17 14	24 20	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	15 15	ns	Fig. 2	

AC WAVEFORMS

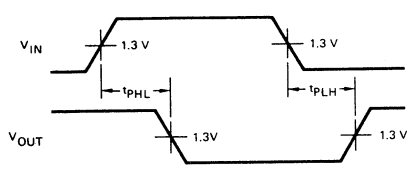


Fig. 1

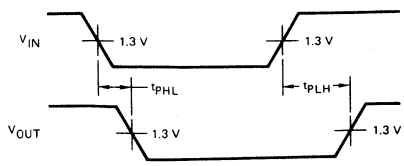


Fig. 2

SN54LS155/SN74LS155
SN54LS156/SN74LS156

DUAL 1-OF-4 DECODER/DEMULTIPLEXER (LS156 HAS OPEN COLLECTOR OUTPUTS)

DESCRIPTION — The LSTTL/MSI SN54LS155/SN74LS155 and SN54LS156/SN74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Motorola TTL families.

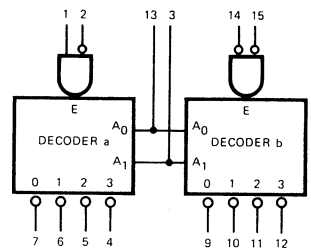
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **COMMON ADDRESS INPUTS**
- **TRUE OR COMPLEMENT DATA DEMULTIPLEXING**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_a$, $\overline{E}_b$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_a	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

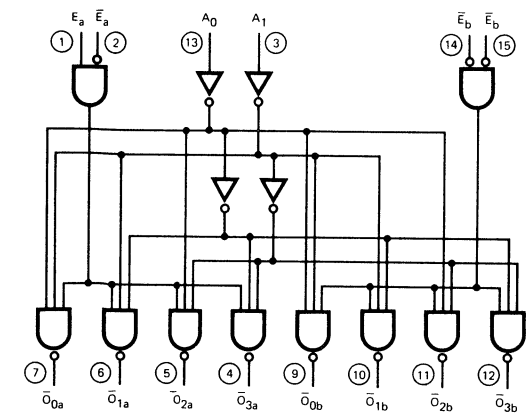
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The HIGH level drive for the LS156 must be established by an external resistor.

LOGIC SYMBOL



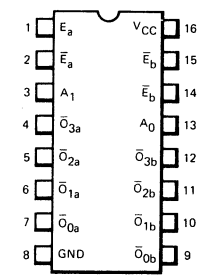
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS155 and LS156 are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$–$\overline{O}_3$). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($E_a \cdot \overline{E}_a$). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the $\overline{E}_a$ or E_a inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection as (A_2). The other $\overline{E}_b$ and $\overline{E}_a$ are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The LS156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \cdot (E + \overline{A}_0 + A_1) \cdot (E + A_0 + \overline{A}_1) \cdot (E + \overline{A}_0 + \overline{A}_1)$$

where $E = E_a + \overline{E}_a$; $E = E_b + E_b$

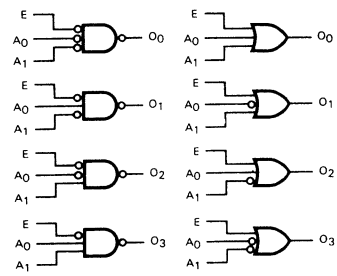


Fig. a

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS155X SN54LS156X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS155X SN74LS156X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage LS155 Only	XM	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.7	3.4			
I_{OH}	Output HIGH Current LS156 Only				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	XM,XC		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		XC		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			6.1	10	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS	
		LS155		LS156				
		TYP	MAX	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Address to Output	11 19	18 27	18 23	28 33	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF $R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}_a$ or $\overline{E}_b$ to Output	9.0 17	15 24	16 21	25 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay E_a to Output	11 20	18 28	18 24	28 34	ns	Fig. 1	

AC WAVEFORMS

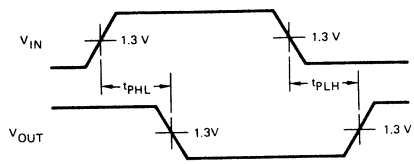


Fig. 1

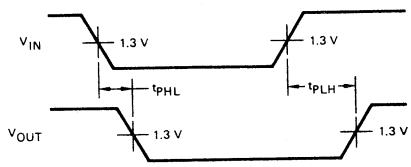


Fig. 2

SN54LS157/SN74LS157

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The LSTTL/MSI SN54LS157/SN74LS157 is a high speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The LS157 can also be used to generate any four of the 16 different functions of two variables. The LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

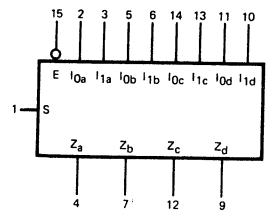
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	10 U.L.	5 (2.5) U.L.

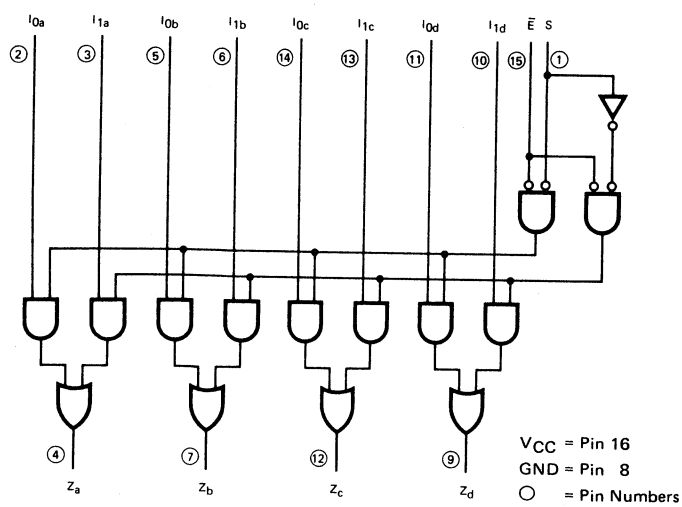
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



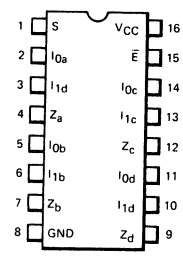
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS157 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S). The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The LS157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the LS157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS157X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS157X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current I_0, I_1				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{E}$, S				40		
	Input HIGH Current at MAX Input Voltage I_0, I_1				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{E}$, S				0.2		
I_{IL}	Input LOW Current I_0, I_1				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{E}$, S				−0.8		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9.7	16	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output			26 24	ns	Fig. 2	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output			25 18	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			14 14	ns	Fig. 2	

AC WAVEFORMS

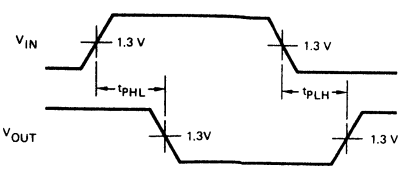


Fig. 1

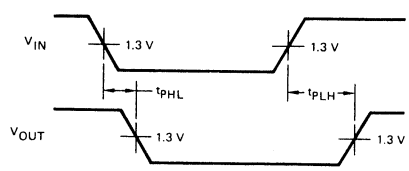


Fig. 2

SN54LS158/SN74LS158

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION – The LSTTL/MSI SN54LS158/SN74LS158 is a high speed Quad 2-Input Multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The LS158 can also generate any four of the 16 different functions of two variables. The LS158 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

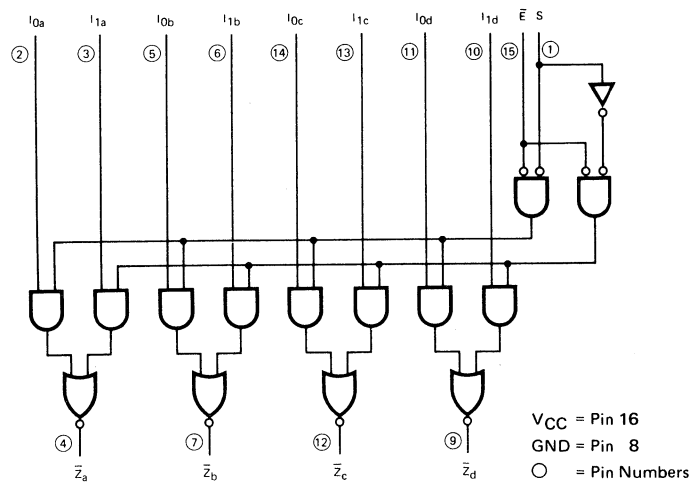
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **INVERTED OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

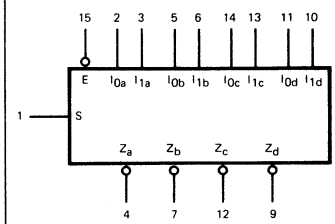
		LOADING (Note a) HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Inverted Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

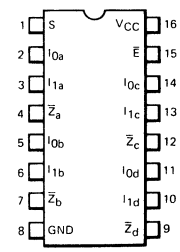


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS158 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S) and presents the data in inverted form at the four outputs. The Enable Input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs.

The LS158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

A common use of the LS158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS158X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS158X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		74	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current I_0, I_1 E, S				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current at MAX Input Voltage I_0, I_1 E, S				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current I_0, I_1 E, S				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			4.8	8.0	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay Select to Output			20 24	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output			21 25	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			13 13	ns	Fig. 1	

AC WAVEFORMS

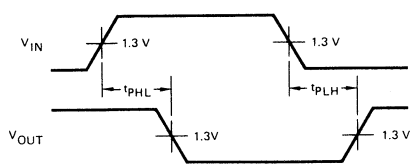


Fig. 1

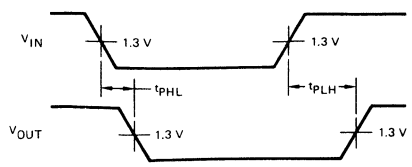


Fig. 2

SN54LS160/SN74LS160 SN54LS161/SN74LS161
SN54LS162/SN74LS162 SN54LS163/SN74LS163

BCD DECADE COUNTERS 4-BIT BINARY COUNTERS

DESCRIPTION — The LS160/161/162/163 are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS160 and LS162 count modulo 10 (BCD). The LS161 and LS163 count modulo 16 (binary.)

The LS160 and LS161 have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162 and LS163 have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS160	LS161
Synchronous Reset	LS162	LS163

- **SYNCHRONOUS COUNTING AND LOADING**
- **TWO COUNT ENABLE INPUTS FOR HIGH SPEED SYNCHRONOUS EXPANSION**
- **TERMINAL COUNT FULLY DECODED**
- **EDGE-TRIGGERED OPERATION**
- **TYPICAL COUNT RATE OF 35 MHz**
- **FULLY TTL AND CMOS COMPATIBLE**

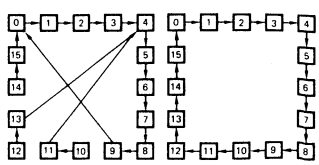
PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.6 U.L.	0.3 U.L.
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.6 U.L.	0.3 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.6 U.L.	0.3 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{SR}$	Synchronous Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commerical (74) Temperature Ranges.

STATE DIAGRAM

LS160 • LS162 LS161 • LS163

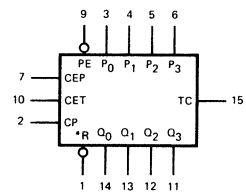


LOGIC EQUATIONS

Count Enable = CEP • CET • PE
TC for LS160 & LS162 = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3
TC for LS161 & LS163 = CET • Q_0 • Q_1 • Q_2 • Q_3
Preset = $\overline{PE}$ • CP+ (rising clock edge)
Reset = $\overline{MR}$ (LS160 & LS161)
Reset = $\overline{SR}$ • CP+ (rising clock edge)
(LS162 & LS163)

NOTE:
The LS160 and LS162 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

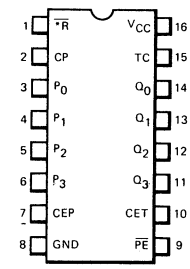
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

*MR for LS160 and LS161
*SR for LS162 and LS163

CONNECTION DIAGRAMS
DIP (TOP VIEW)



*$\overline{MR}$ for LS160 and LS161
*$\overline{SR}$ for LS162 and LS163

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS160/161/162/163 are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. These counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160 and LS161) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs – Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) – select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and $\overline{PE}$ inputs are HIGH. When the $\overline{PE}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the $\overline{PE}$ held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET•CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS160 and LS162 count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do *not* generate a TC output.

The LS161 and LS163 count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the LS160 and LS161 is asynchronous. When the $\overline{MR}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{MR}$ pin should never be left open. If not used, the $\overline{MR}$ pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{SR}$) input of the LS162 and LS163 acts as an edge-triggered control input, overriding CET, CEP, and $\overline{PE}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the LS162 and LS163 only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Enter Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS160X SN54LS161X SN54LS162X SN54LS163X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS160X SN74LS161X SN74LS162X SN74LS163X	4.75 V	5.0 V	5.25 V	0°C to 75°C

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current $P_0 - P_3$, $\overline{MR}$, $\overline{SR}$				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{PE}$, CEP, CP				24		
	CET				40		
	$P_0 - P_3$, MR, SR, PE, CEP CP				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	CET				0.2		
I_{IL}	Input LOW Current $P_0 - P_3$, $\overline{MR}$, $\overline{SR}$				−0.40	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{PE}$, CEP, CP				−0.48		
	CET				−0.80		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Power Supply Current			18	31	mA	V_{CC} = MAX
I_{CCL}				19	32		

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (These parameters apply to all four devices unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Turn Off Delay CP to Q Turn On Delay CP to Q		13 18	20 27	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Turn Off Delay CP to TC Turn On Delay CP to TC		15 14	22 21	ns	Fig. 4	
t_{PLH} t_{PHL}	Turn Off Delay CET to TC Turn On Delay CET to TC		9.0 16	14 23	ns	Fig. 3	
t_{PHL}	Turn On Delay $\overline{MR}$ to Q (LS160 and LS161 Only)		18	28	ns	Fig. 2	
f_{count}	Input Count Frequency	25	35		MHz	Fig. 1	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{rec}	Recovery Time for $\overline{MR}$ (LS160 and LS161 Only)	20			ns	Fig. 2	V_{CC} = 5.0 V
$t_{W\overline{MR}(L)}$	Master Reset Pulse Width (LS160 and LS161 Only)	15	8.0		ns	Fig. 2	
$t_{WCP(H)}$ $t_{WCP(L)}$	Clock Pulse Width (HIGH) Clock Pulse Width (LOW)	15 25	10 18		ns	Fig. 1	
$t_s(H)$ $t_s(L)$	Set-Up Time (HIGH), Data to Clock Set-Up Time (LOW), Data to Clock	20 20			ns	Fig. 5	
$t_h(H)$ $t_h(L)$	Hold Time (HIGH), Data to Clock Hold Time (LOW), Data to Clock	3.0 3.0					
$t_s(H)$ $t_s(L)$	Set-Up Time (HIGH), $\overline{PE}$ or $\overline{SR}$ to Clock Set-Up Time (LOW), $\overline{PE}$ or $\overline{SR}$ to Clock	20 20			ns	Fig. 6	
$t_h(H)$ $t_h(L)$	Hold Time (HIGH), $\overline{PE}$ or $\overline{SR}$ to Clock Hold Time (LOW), $\overline{PE}$ OR $\overline{SR}$ to Clock	0 0					
$t_s(H)$ $t_s(L)$	Set-Up Time (HIGH), CE to Clock Set-Up Time (LOW), CE to Clock	20 20			ns	Fig. 7	
$t_h(H)$ $t_h(L)$	Hold Time (HIGH), CE to Clock Hold Time (LOW), CE to Clock	0 0					

DEFINITION OF TERMS:

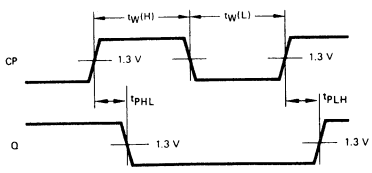
SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

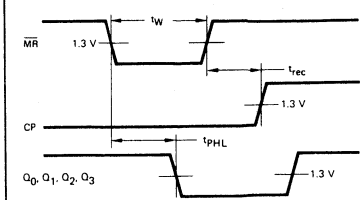
CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.



Other Conditions:
$\overline{PE}$ = $\overline{MR}$ ($\overline{SR}$) = H
CEP = CET = H

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.



Other Conditions:
$\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2

AC WAVEFORMS (Cont'd)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the ($Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) state for the LS160 and LS162 and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the LS161 and LS163.

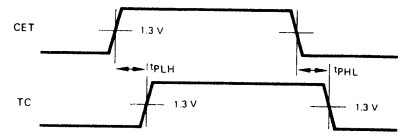


Fig. 3

Other Conditions: CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H

CLOCK TO TERMINAL COUNT DELAYS.

The positive TC pulse is coincident with the output state ($Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3$) for the LS161 and LS163 and ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) for the LS161 and LS163.

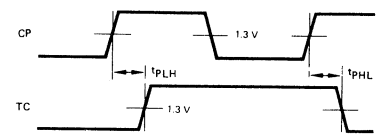


Fig. 4

Other Conditions: $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

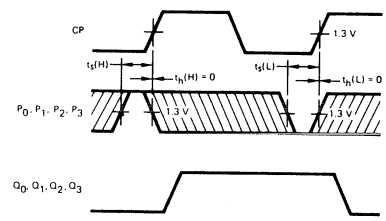


Fig. 5

Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ($\overline{PE}$) INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

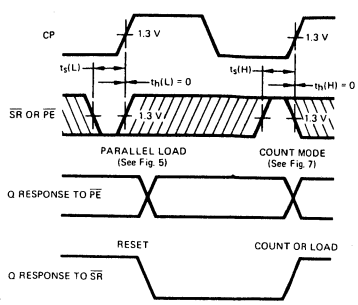
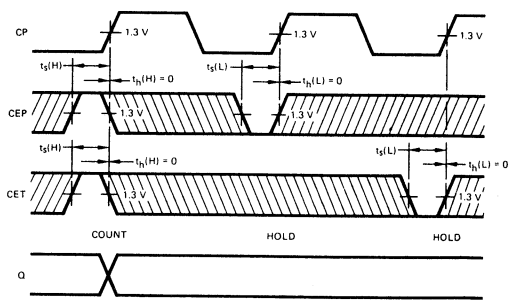


Fig. 6



Other Conditions: $\overline{PE}$ = H, $\overline{MR}$ = H

Fig. 7

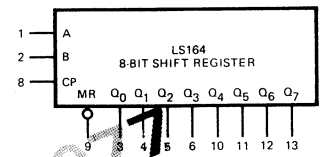
SN54LS164/SN74LS164

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

DESCRIPTION – The SN54LS164/SN74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

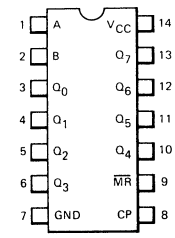
- TYPICAL SHIFT FREQUENCY OF 35 MHz
- ASYNCHRONOUS MASTER RESET
- GATED SERIAL DATA INPUT
- FULLY SYNCHRONOUS DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)

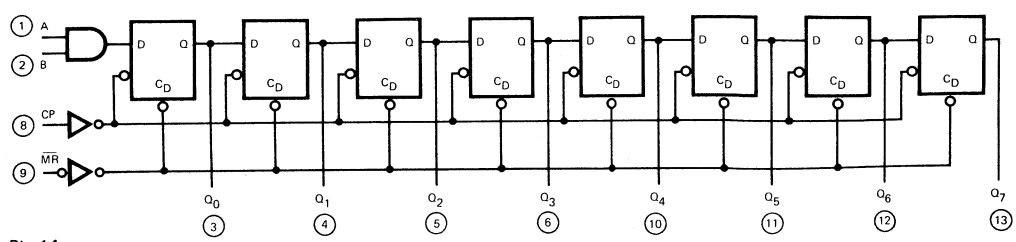


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a) HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A·B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q_0	$Q_1 - Q_7$
Reset (Clear)	L	X	X	L	L – L
Shift	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS164X	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS164X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current (Note 5)			16	27	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.
5. I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Maximum Clock Frequency	25	35		MHz	Fig. 1	V_{CC} = 5 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going Clock to Outputs		17 21	27 32	ns	Fig. 1	
t_{PHL}	Propagation Delay, Negative-Going $\overline{MR}$ to Outputs		24	36	ns	Fig. 2	

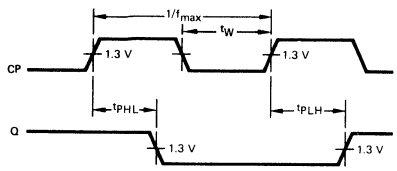
AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_s	Set-Up Time, A or B Input to Positive-Going CP	15			ns	Fig. 3	V_{CC} = 5 V, C_L = 15 pF
t_h	Hold Time, A or B Input to Positive-Going CP	5			ns	Fig. 3	
t_WCP(H)	CP Pulse Width (HIGH)	20			ns	Fig. 1	
t_WCP(L)	CP Pulse Width (LOW)	20			ns	Fig. 1	
$t_W\overline{MR}$(L)	$\overline{MR}$ Pulse Width (LOW)	20			ns	Fig. 2	
t_{rec}	Recovery Time, Positive-Going $\overline{MR}$ to Positive-Going CP	20			ns	Fig. 2	

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: $\overline{MR}$ = H

Fig. 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

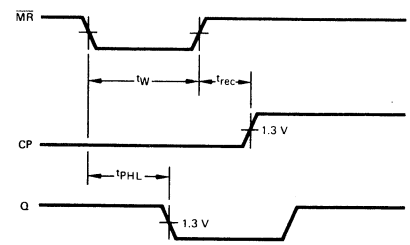


Fig. 2

DATA SET-UP AND HOLD TIMES

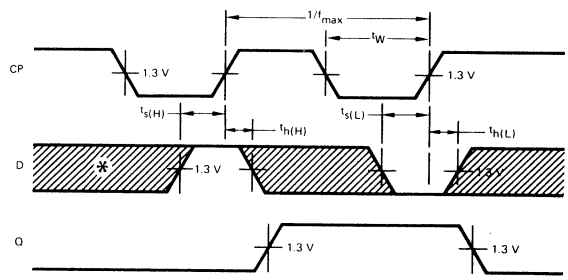


Fig. 3

SN54LS170/SN74LS170

4×4 REGISTER FILE (O/C)

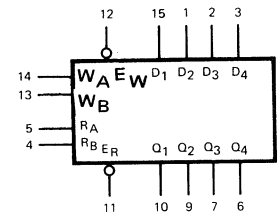
DESCRIPTION — The TTL/MSI SN54LS170/SN74LS170 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

Open collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54LS670/SN74LS670 provides a similar function to this device but it features 3-state outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS OF n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **LOW LEAKAGE OPEN-COLLECTOR OUTPUTS FOR EXPANSION**
- **TYPICAL POWER DISSIPATION OF 125 mW**

LOGIC SYMBOL



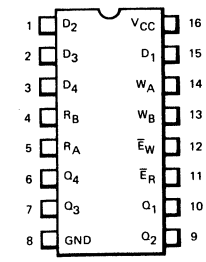
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
W_A, W_B	Write Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_W$	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
R_A, R_B	Read Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_R$	Read Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
Q_1-Q_4	Outputs (Note b)	Open Collector	5(2.5) U.L.

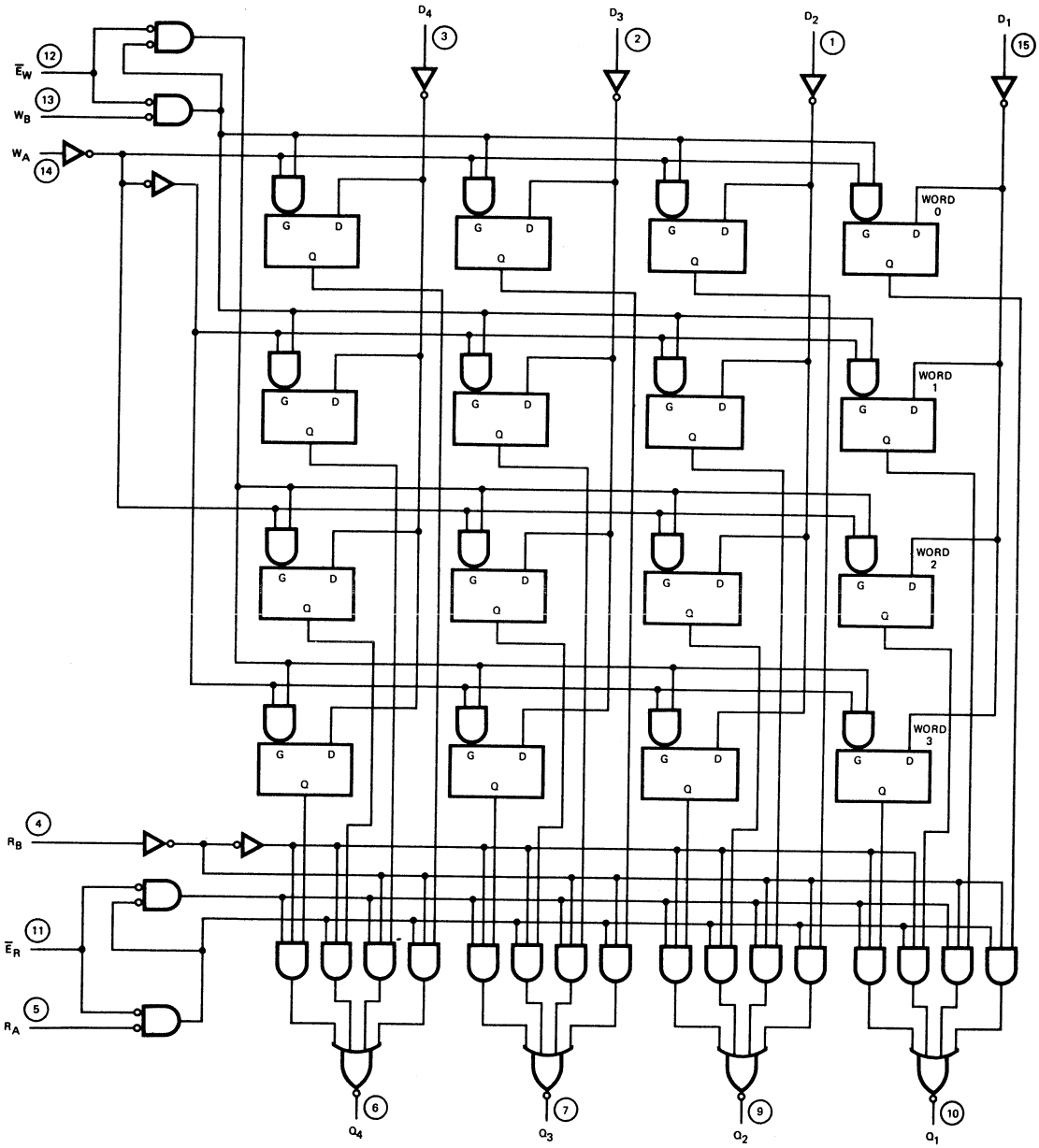
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5.0 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive must be supplied by an external resistor to V_{CC}.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



○ = Pin Numbers
V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS170X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS170X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	(54)			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		(74)			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
I_{OH}	Output HIGH Current				20	μA	V_{OH} = 5.5 V, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current Any D, R, or W				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{E}_R$ or $\overline{E}_W$				40		
	Any D, R, or W				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
	$\overline{E}_R$ or $\overline{E}_W$				0.2		
I_{IL}	Input LOW Current Any D, R or W				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	$\overline{E}_R$ or $\overline{E}_W$				−0.8		
I_{CC}	Power Supply Current (Note 4)			25	40	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{E}_R$ to Q Outputs			30 30	ns	Fig. 1	$V_{CC} = 5$ V $C_L = 15$ pF $R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Q Outputs			40 40	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{E}_W$ to Q Outputs			45 40	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs			45 35	ns	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Pulse Width (LOW) for $\overline{E}_W$	25			ns	$V_{CC} = 5$ V Fig. 3
t_sD (Note 5)	Set-Up Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	10			ns	
t_hD	Hold Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	15			ns	
t_sW (Note 7)	Set-Up Time, Write Select Inputs W_A and W_B with Respect to Negative-Going $\overline{E}_W$	15			ns	
t_hW	Hold Time, Write Select Inputs W_A and W_B with Respect to Positive-Going $\overline{E}_W$	5			ns	

NOTES:
5. The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.
6. The Hold Time (t_h) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.
7. The Address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
8. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

AC WAVEFORMS

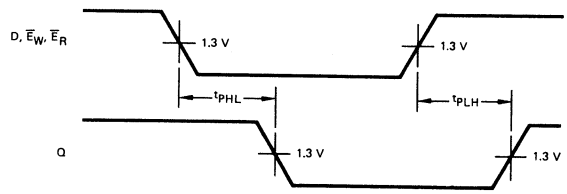


Fig. 1

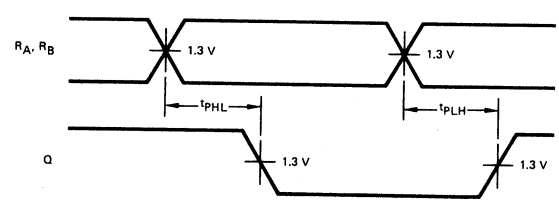


Fig. 2

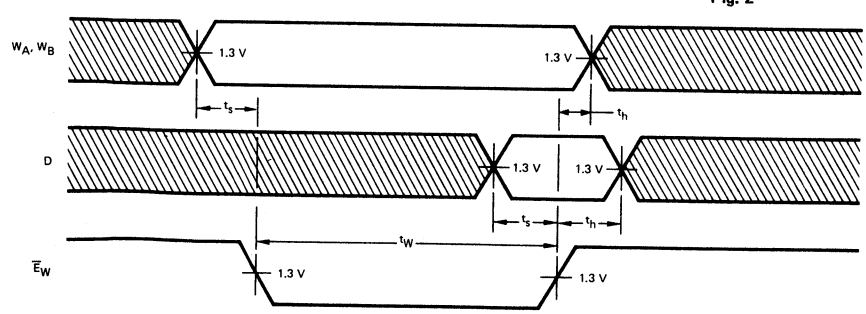


Fig. 3

SN54LS174/SN74LS174

HEX D FLIP-FLOP

DESCRIPTION – The LSTTL/MSI SN54LS174/SN74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

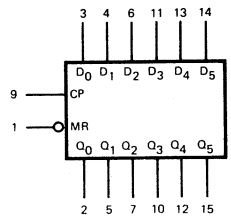
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK**
- **CLOCK TO OUTPUT DELAYS OF 14 ns**
- **ASYNCHRONOUS COMMON RESET**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERNATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_5$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_5$	Outputs (Note b)	10 U.L.	5 (2.5) U.L.

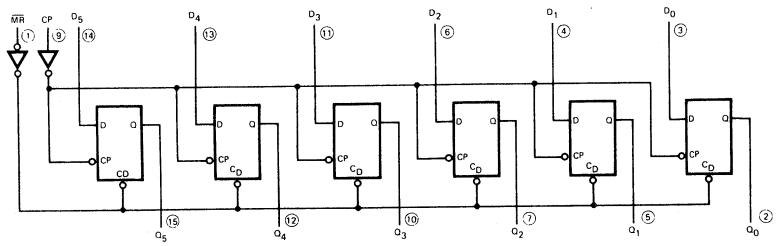
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



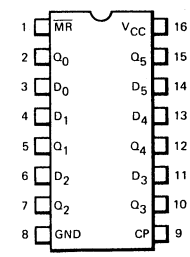
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS174X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS174X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			16	26	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

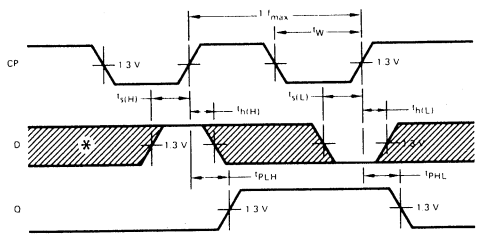
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		12 15	20 22	ns	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		20	28	ns	Fig. 2
f_{MAX}	Maximum Input Clock Frequency	40	55		MHz	Fig. 1

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_WCP	Minimum Clock Pulse Width	15	10		ns	Fig. 1
t_s	Set-up Time, Data to Clock (HIGH or LOW)	10			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	0			ns	Fig. 1
t_{rec}	Recovery Time for $\overline{MR}$	12	8.0		ns	Fig. 2
$t_W\overline{MR}$	Minimum $\overline{MR}$ Pulse Width	12	8.0		ns	Fig. 2

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

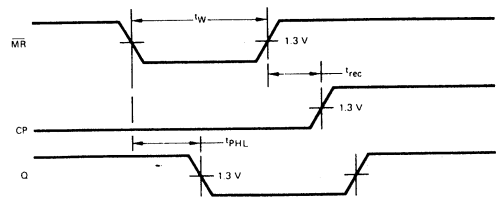


Fig. 2

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SN54LS175/SN74LS175

QUAD D FLIP-FLOP

DESCRIPTION — The LSTTL/MSI SN54LS175/SN74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

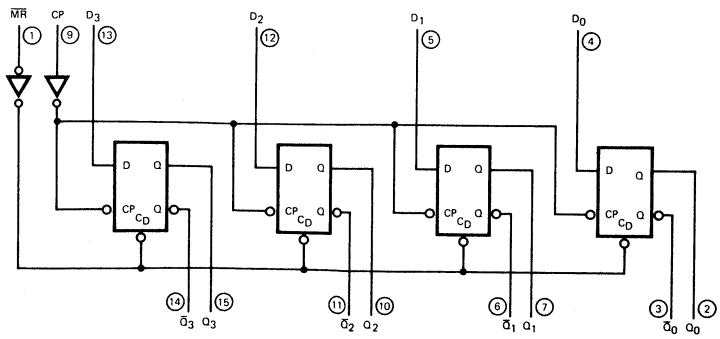
- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED-POSITIVE EDGE-TRIGGERED CLOCK**
- **CLOCK TO OUTPUT DELAYS OF 14 ns**
- **ASYNCHRONOUS COMMON RESET**
- **TRUE AND COMPLEMENT OUTPUT**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_3$	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

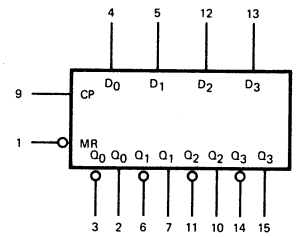
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



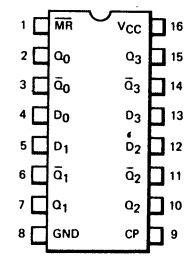
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS175X	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS175X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = –400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				–0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 4)		–15		–100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			11	18	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

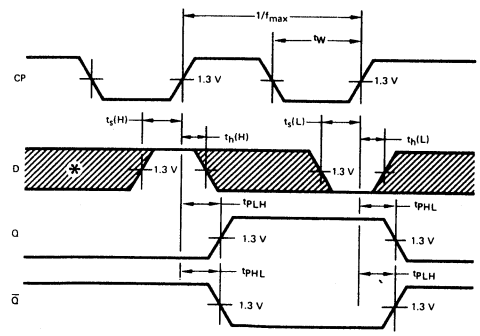
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		12 15	20 22	ns	Fig. 1
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q Output		20	28	ns	Fig. 2
t_{PLH}	Propagation Delay, $\overline{MR}$ to $\overline{Q}$ Output		16	24	ns	Fig. 2
f_{MAX}	Maximum Input Clock Frequency	40	55		MHz	Fig. 1

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_WCP	Minimum Clock Pulse Width	15	10		ns	Fig. 1
t_s	Set-up Time, Data to Clock (HIGH or LOW)	10			ns	Fig. 1
t_h	Hold Time, Data to Clock (HIGH or LOW)	0			ns	Fig. 1
t_{rec}	Recovery Time for $\overline{MR}$	12	8.0		ns	Fig. 2
$t_W\overline{MR}$	Minimum $\overline{MR}$ Pulse Width	12	8.0		ns	Fig. 2

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, CLOCK PULSE WIDTH, FREQUENCY, SET-UP AND HOLD TIMES DATA TO CLOCK



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

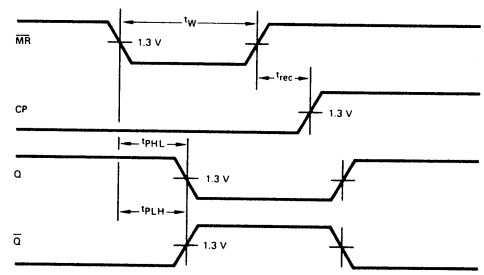


Fig. 2

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SN54LS181/SN74LS181

4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION – The SN54LS181/SN74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE–OR, COMPARE, AND, NAND, OR, NOR, PLUS TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS**
- **INPUT CLAMP DIODES**

PIN NAMES

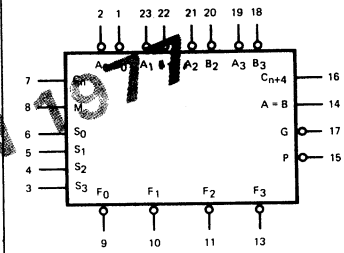
$\overline{A}_0$–$\overline{A}_3$, $\overline{B}_0$–$\overline{B}_3$	Operand (Active LOW) Inputs
S_0–S_3	Function – Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}_0$–$\overline{F}_3$	Function (Active LOW) Outputs
A = B	Comparator Output
$\overline{G}$	Carry Generate (Active LOW) Output
$\overline{P}$	Carry Propagate (Active LOW) Output
C_{n+4}	Carry Output

LOADING (Note a)

HIGH	LOW
1.5 U.L.	0.25 U.L.
2.0 U.L.	1.0 U.L.
0.5 U.L.	0.25 U.L.
2.5 U.L.	1.25 U.L.
10 U.L.	5 (2.5) U.L.
Open Collector	5 (2.5) U.L.
10 U.L.	10 U.L.
10 U.L.	5 U.L.
10 U.L.	5 (2.5) U.L.

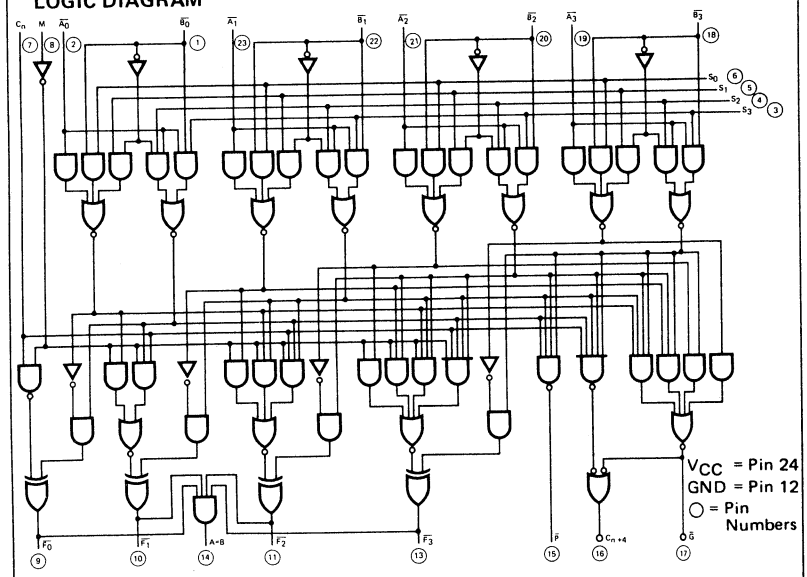
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



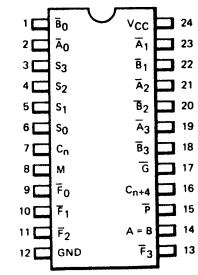
V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
○ = Pin Numbers

CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL DESCRIPTION — The SN54LS181/SN74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the $\overline{C}_{n+4}$ output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the LS181 goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3 S_2 S_1 S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L L H L	$\overline{A + B}$	$A\overline{B}$ minus 1	$\overline{AB}$	A + $\overline{B}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A + B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L H H H	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$	AB minus 1
H L L L	$\overline{A}B$	A plus (A + B)	$\overline{A + B}$	A plus AB
H L L H	A ⊕ B	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	$A\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H H H L	AB	$A\overline{B}$ plus A	A + B	(A + $\overline{B}$) plus A
H H H H	A	A	A	A minus 1

L = LOW Voltage Level

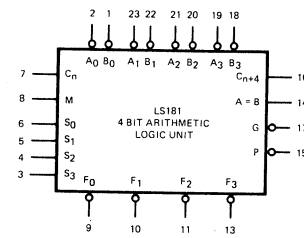
H = HIGH Voltage Level

*Each bit is shifted to the next more significant position

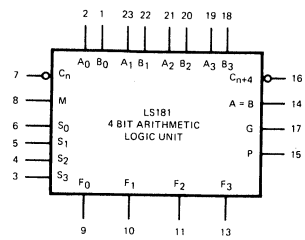
**Arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS181X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS181X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
	Any Output except A=B	74	2.7	3.4			V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{OH}	Output HIGH Current A=B Output Only				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage Except $\overline{G}$ and $\overline{P}$	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
	Output LOW Voltage Output $\overline{G}$			0.47	0.7	V	I_{OL} = 16 mA
	Output LOW Voltage Output $\overline{P}$	54		0.35	0.6	V	I_{OL} = 8.0 mA
		74		0.35	0.7		
I_{IH}	Input HIGH Current Mode Input $\overline{A}$ and $\overline{B}$ Inputs S Inputs Carry Inputs				20 60 80 100	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Mode Input $\overline{A}$ and $\overline{B}$ Inputs S Inputs Carry Inputs				0.1 0.3 0.4 0.5	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current Mode Input $\overline{A}$ and $\overline{B}$ Inputs S Inputs Carry Inputs				−0.36 −1.08 −1.44 −2.0	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current Condition A (Note 5)	54		20	32	mA	V_{CC} = MAX
		74		20	34		
	Power Supply Current Condition B (Note 5)	54		21	35		
		74		21	37		

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.
5. With outputs open, I_{CC} is measured for the following conditions:
   A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
   B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, Pin 12 = GND

SYMBOL	PARAMETER	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})		27 20	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I and II
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ Outputs)		26 20	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		29 23	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		32 26	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		30 30	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		30 33	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Output)		32 20	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to any $\overline{F}$ Output)		32 23	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{F}$ Outputs)		33 29	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		38 38	ns	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		41 41	ns	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode)
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to A = B Output)		50 62	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V, R_L = 2 kΩ (Diff Mode) See Fig. 5 and Table II

AC WAVEFORMS

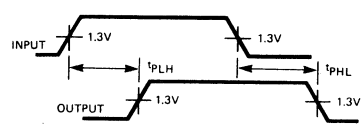


Fig. 4

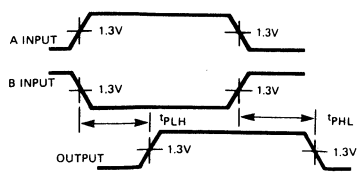


Fig. 5

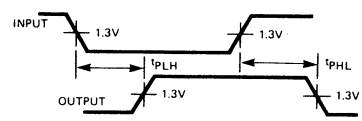


Fig. 6

SUM MODE TEST TABLE I — **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or $C_n + 4$

DIFF MODE TEST TABLE II — **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_2 = M = 4.5$ V $S_0 = S_3 = 0$ V

SN54LS190/ SN74LS190
PRESETTABLE BCD/DECADE UP/DOWN COUNTERS

SN54LS191/ SN74LS191
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

DESCRIPTION – The SN54LS190/SN74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the SN54LS191/SN74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load ($\overline{PL}$) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable ($\overline{CE}$) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control ($\overline{U}/D$) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock ($\overline{RC}$) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

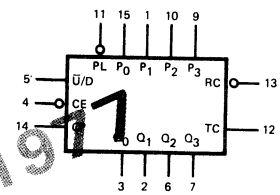
- LOW POWER . . . 90 mW TYPICAL DISSIPATION
- HIGH SPEED . . . 35 MHz TYPICAL COUNT FREQUENCY
- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PARALLEL LOAD
- INDIVIDUAL PRESET INPUTS
- COUNT ENABLE AND UP/DOWN CONTROL INPUTS
- CASCADABLE
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CE}$	Count Enable (Active LOW) Input	1.5 U.L.	0.7 U.L.
CP	Clock Pulse (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{U}/D$	Up/Down Count Control Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Parallel Load Control (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{RC}$	Ripple Clock Output (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

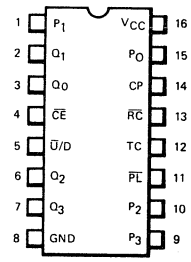
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



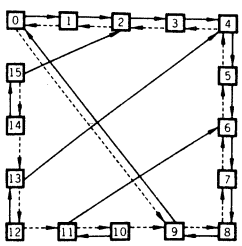
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS



190

LS190

UP: $TC = Q_0 \cdot Q_3 \cdot (\overline{U/D})$

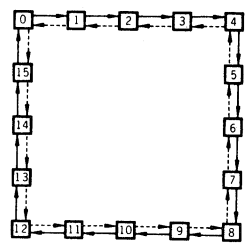
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U/D})$

LS191

UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\overline{U/D})$

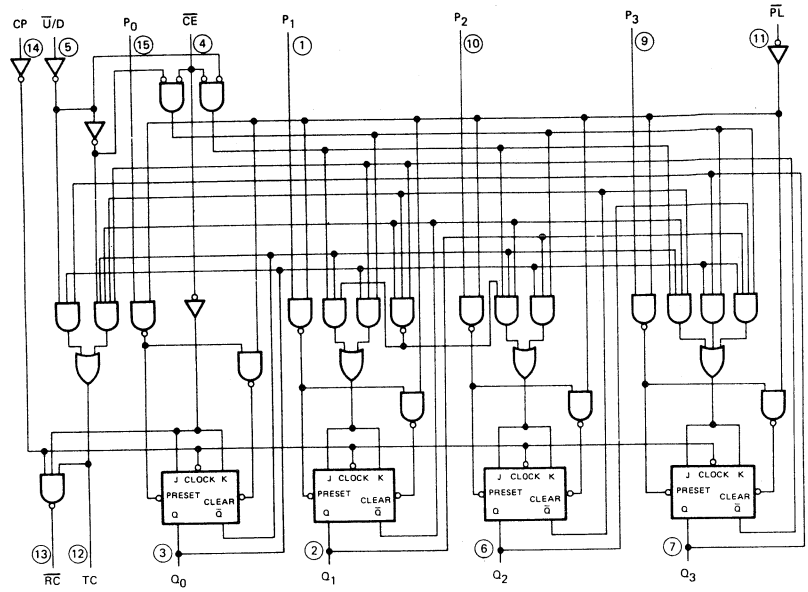
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (\overline{U/D})$

Count Up ——
Count Down ------

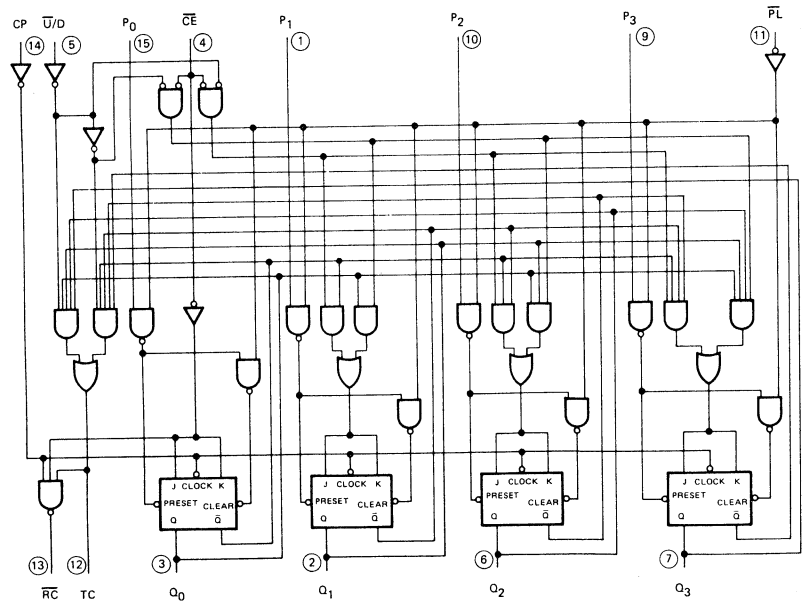


191

LOGIC DIAGRAMS



DECADE COUNTER
LS190



BINARY COUNTER
LS191

V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Numbers

FUNCTIONAL DESCRIPTION – The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the $\overline{CE}$ signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Similarly, the $\overline{U}$/D signal should only be changed when either $\overline{CE}$ or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			$\overline{RC}$
$\overline{CE}$	TC*	CP	OUTPUT
L	H	⎍⎍	⎍⎍
H	X	X	H
X	L	X	H

*TC is generated internally

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH Clock Transition
⎍⎍ = LOW Pulse

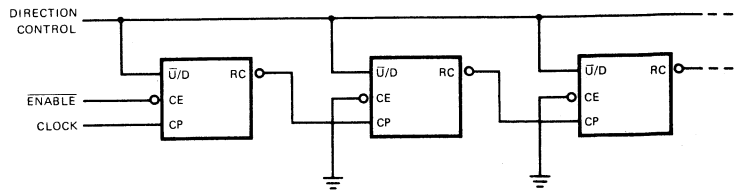


Fig. a) n-stage counter using ripple clock.

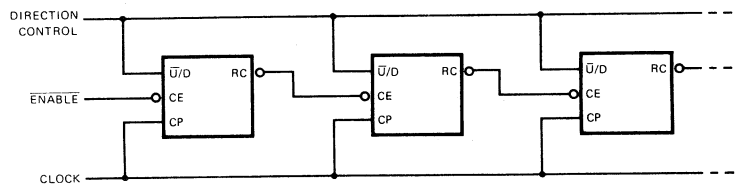


Fig. b) Synchronous n-stage counter using ripple carry/borrow.

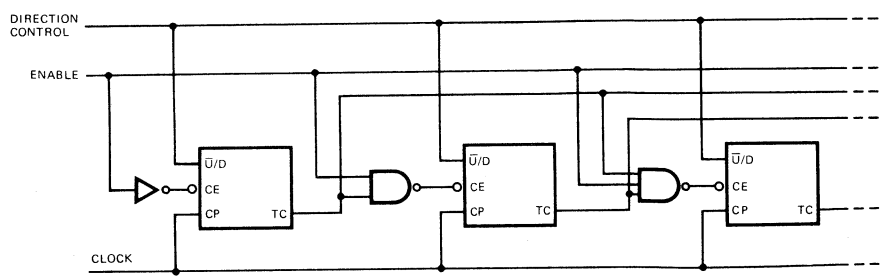


Fig. c) Synchronous n-stage counter with parallel gated carry/borrow.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS190X SN54LS191X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS190X SN74LS191X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current P_n, $\overline{PL}$, CP, $\overline{U}/D$, $\overline{CE}$				20 60	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	P_n, $\overline{PL}$, CP, $\overline{U}/D$, $\overline{CE}$				0.1 0.3	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current P_n, $\overline{PL}$, CP, $\overline{U}/D$, $\overline{CE}$				−0.4 −1.08	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			20	35	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.
5. The Set-Up Time "t_s(H)" and Hold Time "t_h(L)" between the Count Enable ($\overline{CE}$) and the Clock (CP) indicate that the LOW-to-HIGH transition of the $\overline{CE}$ must occur only while the Clock is HIGH for conventional operation.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Max. Input Count Frequency	25	35		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, CP Input to Q Outputs			24 36	ns	Fig. 1	
t_{PLH} t_{PHL}	CP Input to $\overline{RC}$ Output			20 24	ns	Fig. 2	
t_{PLH} t_{PHL}	CP Input to TC Output			42 52	ns	Fig. 1	
t_{PLH}* t_{PHL}*	$\overline{U}$/D Input to $\overline{RC}$ Output			45 45	ns	Fig. 7	
t_{PLH} t_{PHL}	$\overline{U}$/D Input to TC Output			33 33	ns		
t_{PLH} t_{PHL}	$P_0 - P_3$ Inputs to $Q_0 - Q_3$ Outputs			22 50	ns	Fig. 3	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output			33 50	ns	Fig. 4	
t_{PLH}* t_{PHL}	$\overline{CE}$ Input to $\overline{RC}$ Output			33 33	ns	Fig. 2	

*It is possible to get these timing relationships, but they should not occur during normal operation since the CP would be HIGH.

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_W	CP Pulse Width	20			ns	Fig. 1	V_{CC} = 5.0 V
t_W	$\overline{PL}$ Pulse Width	35			ns	Fig. 4	
t_sL	Set-Up Time LOW, Data to $\overline{PL}$	20			ns	Fig. 6	
t_hL	Hold Time LOW, Data to $\overline{PL}$	0			ns		
t_sH	Set-Up Time HIGH, Data to $\overline{PL}$	20			ns		
t_hH	Hold Time HIGH, Data to $\overline{PL}$	0			ns		
t_{rec}	Recovery Time, $\overline{PL}$ to CP	20			ns	Fig. 5	
t_sL	Set-Up Time LOW, $\overline{CE}$ to Clock	20			ns	Fig. 8	
t_hL	Hold Time LOW, $\overline{CE}$ to Clock	0			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

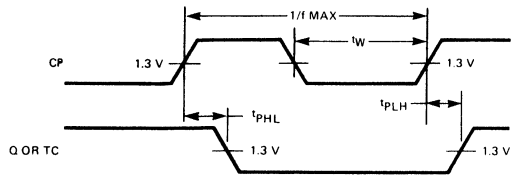


Fig. 1

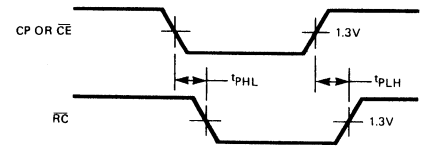
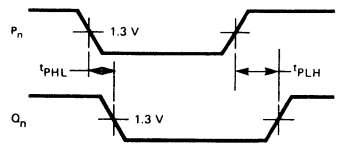


Fig. 2



NOTE: $\overline{PL}$ = LOW

Fig. 3

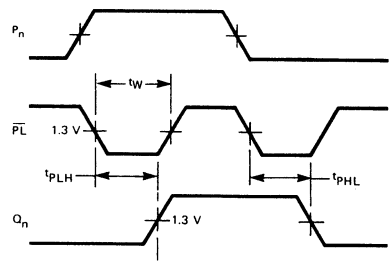


Fig. 4

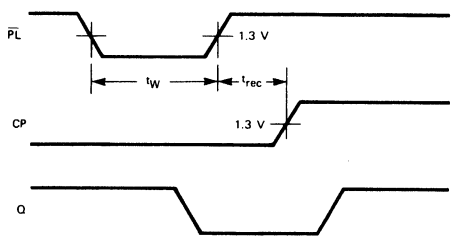
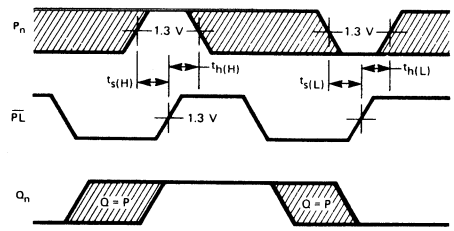


Fig. 5



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

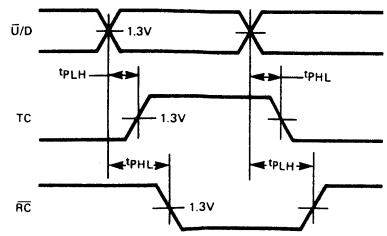


Fig. 7

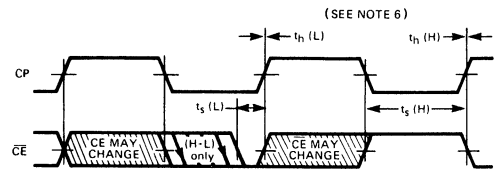


Fig. 8

SN54LS192/ SN74LS192

PRESETTABLE BCD/DECADE UP/DOWN COUNTER

SN54LS193/ SN74LS193

PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

DESCRIPTION – The SN54LS192/SN74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54LS193/SN74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

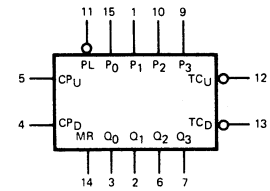
- **LOW POWER . . . . 95 mW TYPICAL DISSIPATION**
- **HIGH SPEED . . . 40 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD**
- **INDIVIDUAL PRESET INPUTS**
- **CASCADING CIRCUITRY INTERNALLY PROVIDED**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP_U	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.
CP_D	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.
MR	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5(2.5) U.L.
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5(2.5) U.L.

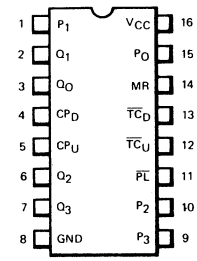
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for MILITARY (54) and 5 U.L. for COMMERCIAL (74) Temperature Ranges.

LOGIC SYMBOL



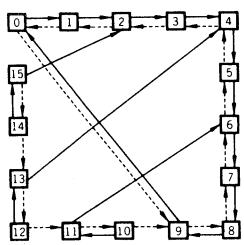
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS



LS192

LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

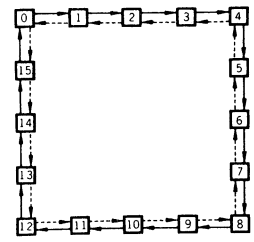
LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

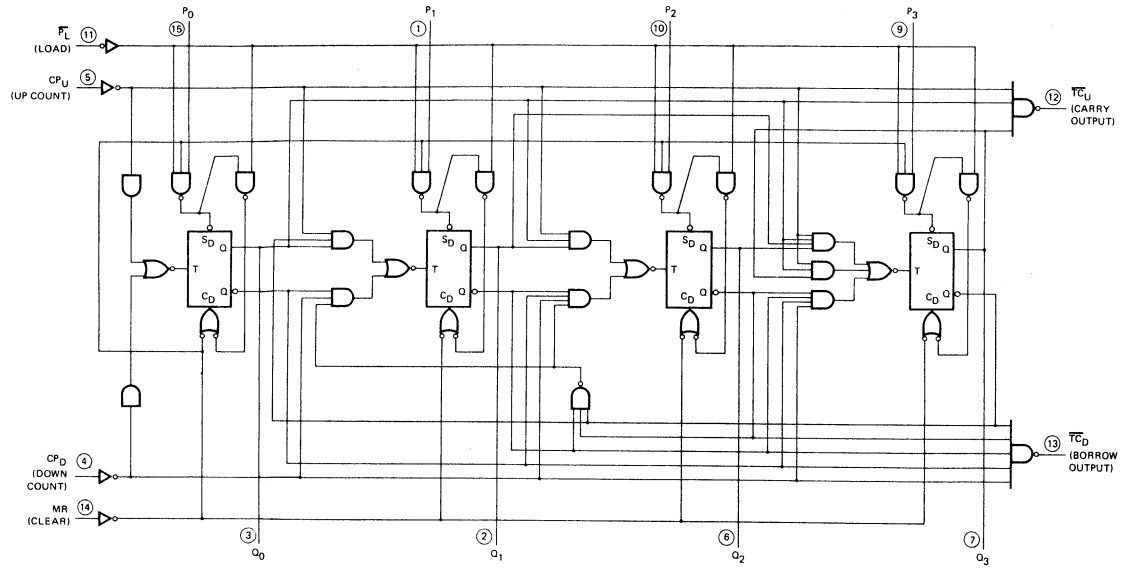
COUNT UP ——

COUNT DOWN ------

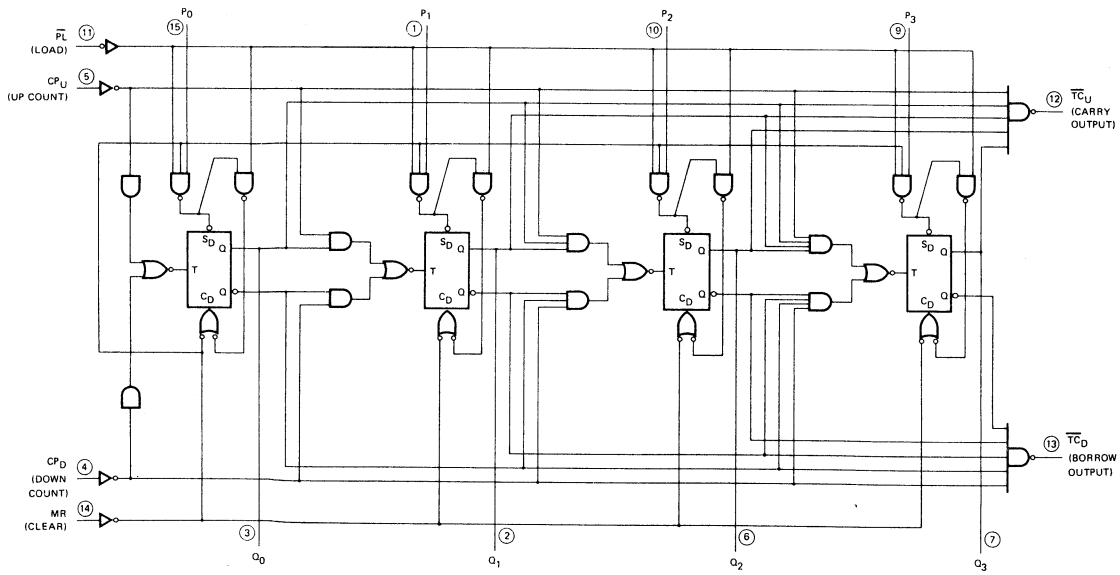


LS193

LOGIC DIAGRAMS



LS192



LS193

V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Number

FUNCTIONAL DESCRIPTION – The LS192 and LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 5 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asnyn.)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0 V
* Input Voltage (dc)	−0.5 V to 15 V
* Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

* Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS192X SN54LS193X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS192X SN74LS193X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			19	34	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, now shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		LS192			LS193					
		MIN	TYP	MAX	MIN	TYP	MAX			
f_{MAX}	Max Input Count Frequency	30	40		30	40		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	CP_U Input to $\overline{TC}_U$ Output		10 14	16 21		10 14	16 21	ns	Fig. 2	
t_{PLH} t_{PHL}	CP_D Input to $\overline{TC}_D$ Output		10 15	16 22		10 15	16 22	ns		
t_{PLH} t_{PHL}	CP_U or CP_D to Q_n Outputs		22 18	31 28		22 18	31 28	ns		
t_{PLH} t_{PHL}	$P_0 - P_3$ Inputs $Q_0 - Q_3$ Outputs							ns	Fig. 3	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		23 17	32 25		23 17	32 25	ns	Fig. 4	
t_{PHL}	MR Input to Any Output		17	25		17	25	ns	Fig. 7	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		LS192			LS193					
		MIN	TYP	MAX	MIN	TYP	MAX			
t_W	CP_U Pulse Width	17			17			ns	Fig. 1	V_{CC} = 5.0 V
t_W	CP_D Pulse Width	17			17			ns		
t_W	$\overline{PL}$ Pulse Width	15			15			ns	Fig. 4	
t_W	MR Pulse Width	15			15			ns	Fig. 7	
t_sL	Set-up Time LOW, Data to $\overline{PL}$	10			10			ns	Fig. 6	
t_hL	Hold Time LOW, Data to $\overline{PL}$	0			0			ns		
t_sH	Set-up Time HIGH, Data to $\overline{PL}$	10			10			ns		
t_hH	Hold Time HIGH, Data to $\overline{PL}$	0			0			ns		
t_{rec}	Recovery Time, $\overline{PL}$ to CP							ns	Fig. 5	
t_{rec}	Recovery Time, MR to CP							ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the $\overline{PL}$ transistion from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the $\overline{PL}$ transistion from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the $\overline{PL}$ transistion from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

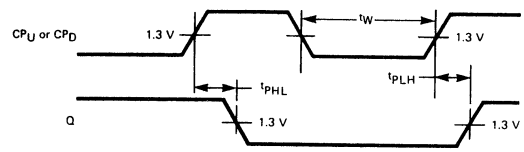


Fig. 1

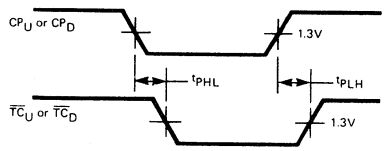
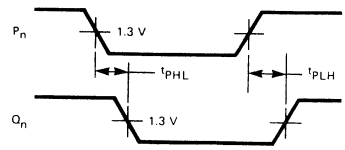


Fig. 2



NOTE: $\overline{PL}$ = LOW

Fig. 3

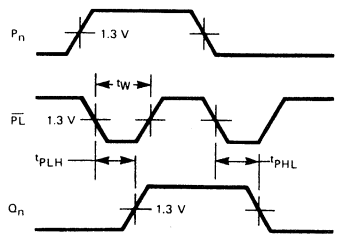


Fig. 4

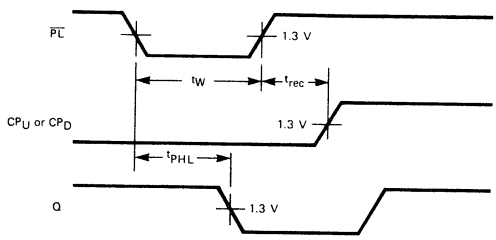
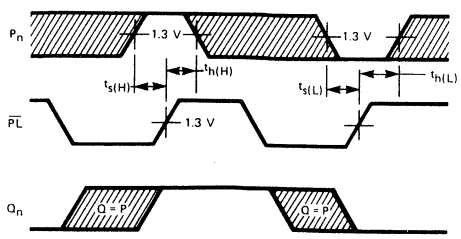


Fig. 5



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6

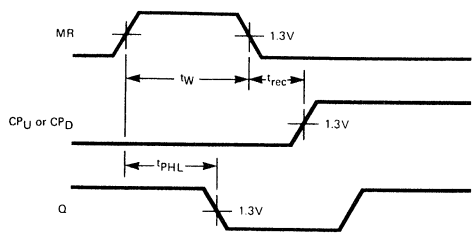


Fig. 7

SN54LS194A/SN74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION — The SN54LS194A/SN74LS194A is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194 is similar in operation to the LS195 Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL families.

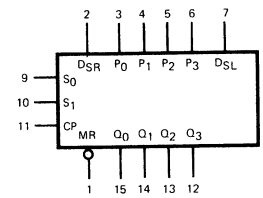
- **TYPICAL SHIFT FREQUENCY OF 40 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **HOLD (DO NOTHING) MODE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
S_0, S_1	Mode Control Inputs	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
D_{SR}	Serial (Shift Right) Data Input	0.5 U.L.	0.25 U.L.
D_{SL}	Serial (Shift Left) Data Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.

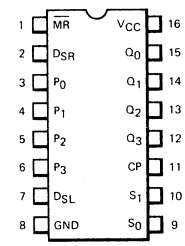
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

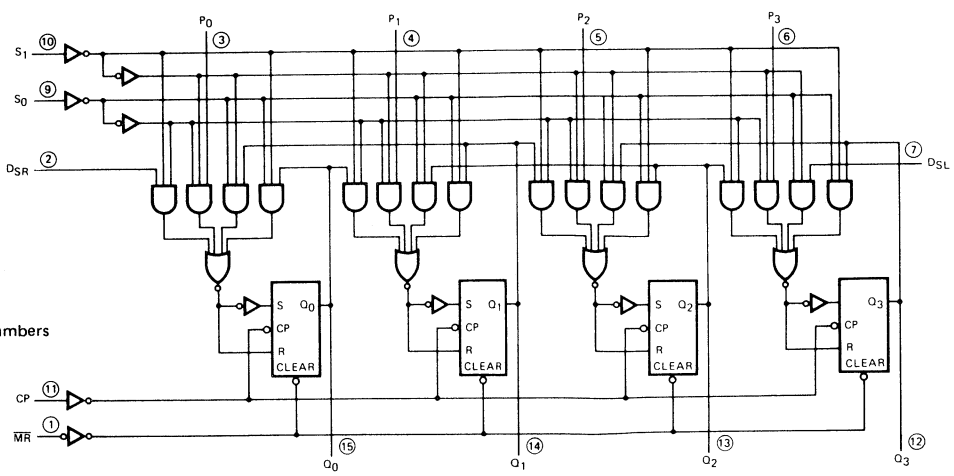


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The Logic Diagram and Truth Table indicate the functional characteristics of the LS194 4-Bit Bidirectional Shift Register. The LS194 is similar in operation to the Motorola LS195 Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

1. All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

2. The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.

3. The four parallel data inputs (P_0, P_1, P_2, P_3) are D-type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0, P_1, P_2, and P_3 inputs is transferred to the Q_0, Q_1, Q_2, and Q_3 outputs respectively following the next LOW to HIGH transition of the clock.

4. The asynchronous Master Reset ($\overline{MR}$), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194 design which increase the range of application are described below:

1. Two mode control inputs (S_0, S_1) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.

2. D-type serial data inputs (D_{SR}, D_{SL}) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

L = LOW Voltage Level
H= HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS194AX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS194AX	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			15	23	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			22 15	ns	Fig. 1	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output			18	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_W(CP)	Clock Pulse Width	18	12		ns	Fig. 1	V_{CC} = 5.0 V
t_s(Data)	Set-up Time, Data to Clock	16			ns	Fig. 3	
t_h(Data)	Hold Time, Data to Clock	0			ns		
t_s(S)	Set-up Time, Mode Control to Clock	20			ns	Fig. 4	
t_h(S)	Hold Time, Mode Control to Clock	0			ns		
t_W(MR)	Master Reset Pulse Width	12			ns	Fig. 2	
t_{rec}(MR)	Recovery Time Master Reset to Clock	18	12		ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

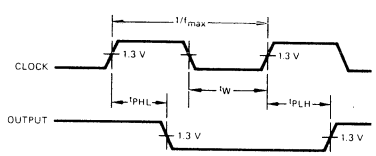
HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

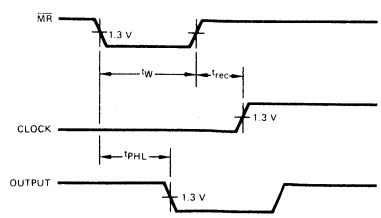
CLOCK TO OUTPUT DELAYS CLOCK PULSE WIDTH AND f_{max}



OTHER CONDITIONS: S_1 = L, $\overline{MR}$ = H, S_0 = H

Fig. 1

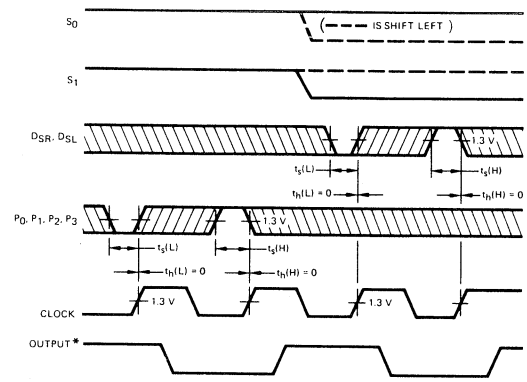
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



OTHER CONDITIONS: S_0, S_1 = H
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2

SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (D_{SR}, D_{SL}) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



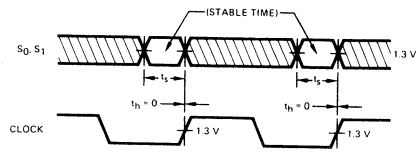
OTHER CONDITIONS: $\overline{MR}$ = H

*D_{SR} set-up time affects Q_0 only

D_{SL} set-up time affects Q_3 only

Fig. 3

SET-UP (t_s) AND HOLD (t_h) TIME FOR S INPUT



OTHER CONDITIONS: $\overline{MR}$ = H

Fig. 4

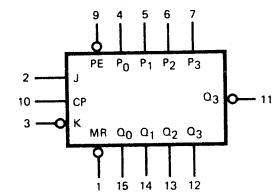
SN54LS195A/SN74LS195A

UNIVERSAL 4-BIT SHIFT REGISTER

DESCRIPTION – The SN54LS195A/SN74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 50 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- TYPICAL SHIFT RIGHT FREQUENCY OF 50 MHz
- ASYNCHRONOUS MASTER RESET
- J, $\overline{K}$ INPUTS TO FIRST STAGE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



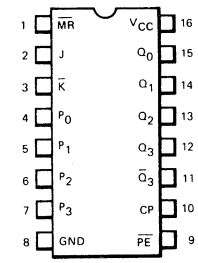
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note b)	10 U.L.	5(2.5) U.L.

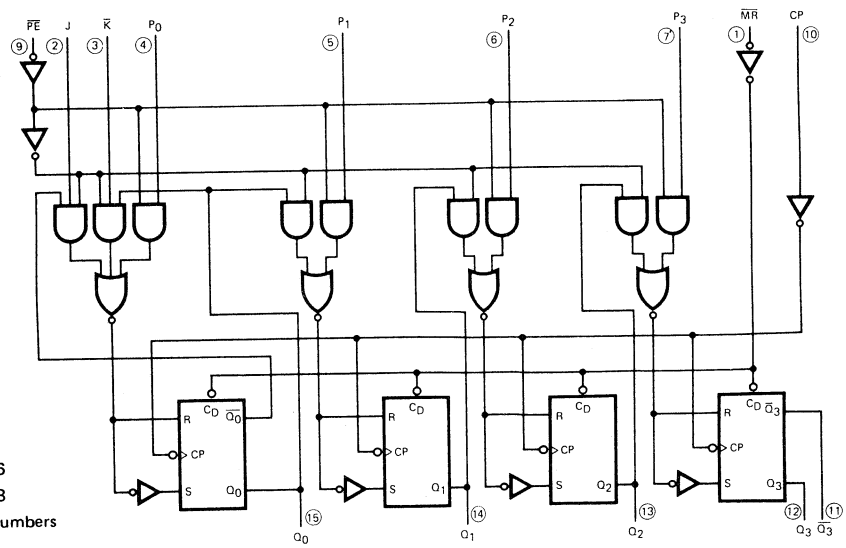
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The Logic Diagram and Truth Table indicate the functional characteristics of the LS195 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195 has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW to HIGH clock transition. The $J\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins togethers. When the $\overline{PE}$ input is LOW, the LS195 appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW to HIGH clock transition. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occuring after each LOW to HIGH clock transition. Since the LS195 utilizes edge-triggering, there is no restriction on the activity of the J, $\overline{K}$, P_n and $\overline{PE}$ inputs for logic operation – except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT – TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p}_3$

L = LOW voltage levels
H = HIGH voltage levels
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS195AX	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS195AX	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			14	21	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	40		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		14 13	21 20	ns	Fig. 1	
t_{PHL}	Propagation Delay, MR to Output		13	20	ns	Fig. 3	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_W(CP)	Clock Pulse Width	16			ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_s(Data)	Set-up Time, Data to Clock	15	8		ns	Fig. 2	
t_h(Data)	Hold Time, Data to Clock	0	−7		ns		
$t_s(\overline{PE})$	Set-up Time, $\overline{PE}$ Control to Clock	25	18		ns	Fig. 4	
$t_h(\overline{PE})$	Hold Time, $\overline{PE}$ Control to Clock	−10	−17		ns		
$t_W(\overline{MR})$	Master Reset Pulse Width	12			ns	Fig. 3	
$t_{rec}(\overline{MR})$	Recovery Time Master Reset to Clock	25			ns		

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

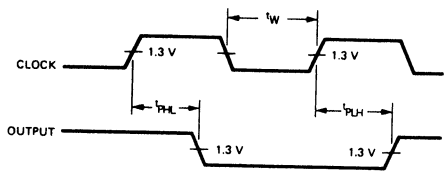
HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

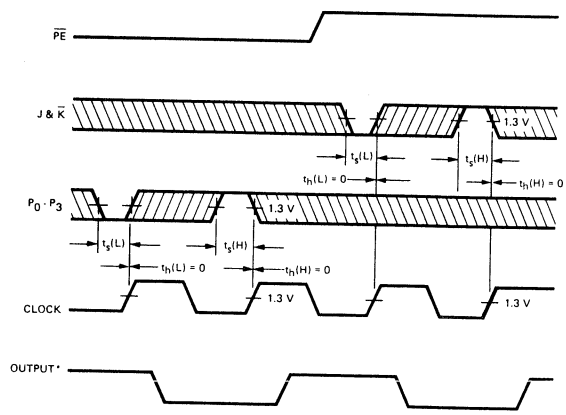
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



CONDITIONS: $J = \overline{PE} = \overline{MR} = H$
$\overline{K} = L$

Fig. 1

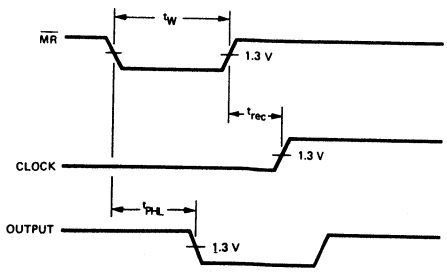
SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & $\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



CONDITIONS: $\overline{MR} = H$
*J and $\overline{K}$ set-up time affects Q_0 only

Fig. 2

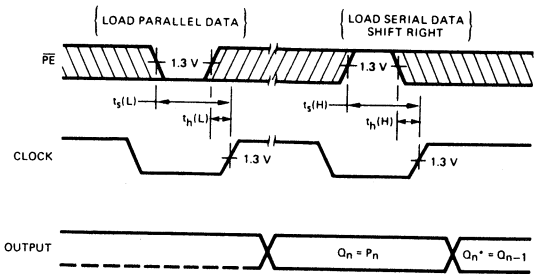
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



CONDITIONS: $\overline{PE} = L$
$P_0 = P_1 = P_2 = P_3 = H$

Fig. 3

SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT



CONDITIONS: $\overline{MR} = H$
*Q_0 state will be determined by J and $\overline{K}$ inputs

Fig. 4

SN54LS196/SN74LS196
SN54LS197/SN74LS197

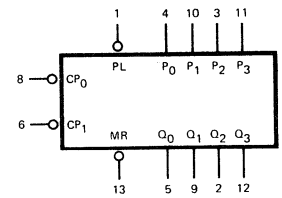
4-STAGE PRESETTABLE RIPPLE COUNTERS

DESCRIPTION – The SN54LS196/SN74LS196 decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8,4,2,1) sequence or in a bi-quinary mode producing a 50% duty cycle output. The SN54LS197/SN74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH.

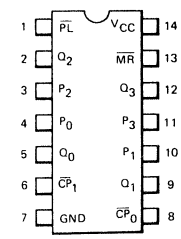
- LOW POWER CONSUMPTION – TYPICALLY 80 mW
- HIGH COUNTING RATES – TYPICALLY 70 MHz
- CHOICE OF COUNTING MODES – BCD, BI-QUINARY, BINARY
- ASYNCHRONOUS PRESETTABLE
- ASYNCHRONOUS MASTER RESET
- EASY MULTISTAGE CASCADING
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)

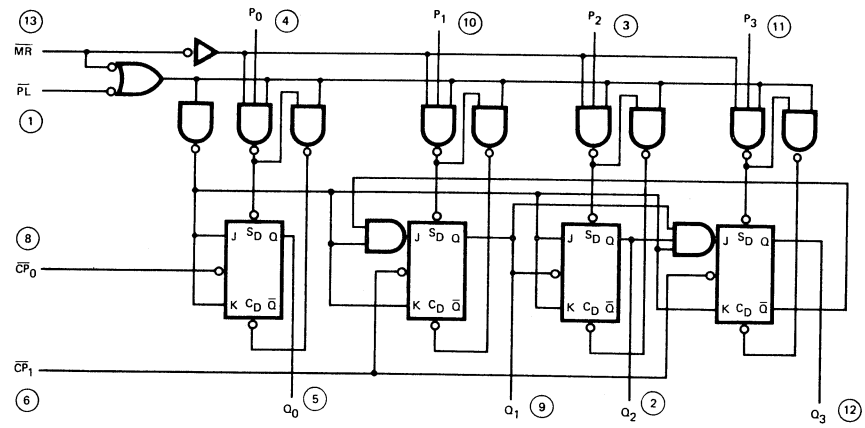


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

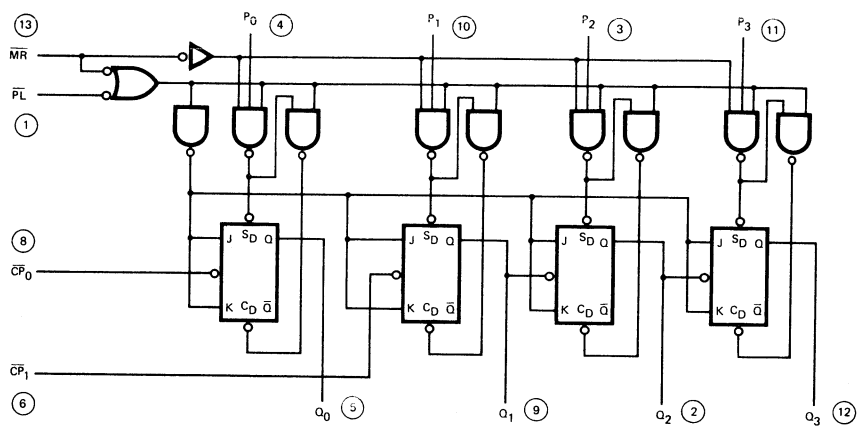
PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to Divide-by-Two Section	1.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Five Section	2.0 U.L.	1.75 U.L.
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to Divide-by-Eight Section	1.0 U.L.	1.0 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{PL}$	Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_0-P_3	Data Inputs	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Outputs (Notes b, c)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c. In addition to loading shown, Q_0 can also drive $\overline{CP}_1$.

LOGIC DIAGRAM



LS196



LS197

V_{CC} = Pin 14
GND = Pin 7
○ = Pin Numbers

FUNCTIONAL DESCRIPTION — The LS196 and LS197 are asynchronously presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP_0}$ input serves the Q_0 flip-flop in both circuit types while the $\overline{CP_1}$ input serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP_1}$ input. With the input frequency connected to $\overline{CP_0}$ and Q_0 driving $\overline{CP_1}$, the LS197 forms a straightforward module-16 counter, with Q_0 the least significant output and Q3 the most significant output.

The LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to $\overline{CP_0}$ and with Q_0 driving $\overline{CP_1}$, the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to $\overline{CP_1}$ and Q_3 driving $\overline{CP_0}$, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data ($P_0 - P_3$) inputs into the flip-flops. While PL is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs.

Figure 2: LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES:
1. Signal applied to CP_0, Q_0 connected to CP_1.
2. Signal applied to CP_1, Q_3 connected to CP_0.

MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	⌐	Count

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = HIGH to Low Clock Transition

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS196X SN54LS197X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS196X SN74LS197X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$ (LS197) $\overline{CP_1}$ (LS196)				20 40 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	$\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$ (LS197) $\overline{CP_1}$ (LS196)				0.1 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current $\overline{PL}$, P_0, P_1, P_2, P_3 $\overline{MR}$ $\overline{CP_0}$ $\overline{CP_1}$ (LS196) $\overline{CP_1}$ (LS197)				−0.36 −0.72 −2.4 −2.8 −1.3	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			12	20	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		LS196			LS197					
		MIN	TYP	MAX	MIN	TYP	MAX			
f_{max}	Input Count Frequency	45	60		50	75		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	$\overline{CP_0}$ Input to Q_0 Output		8.0 8.0	12 12		8.0 8.0	12 12	ns	Fig. 1	
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_1 Output		9.0 9.0	14 14		9.0 9.0	14 14	ns		
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_2 Output		23 21	34 32		26 23	36 34	ns		
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_3 Output		12 12	18 18		35 38	50 55	ns		
t_{PLH} t_{PHL}	P_0, P_1, P_2, P_3 Inputs Q_0, Q_1, Q_2, Q_3 Outputs		10 24	15 35		10 24	15 35	ns	Fig. 2	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		15 24	24 35		15 24	24 35	ns	Fig. 3	
t_{PHL}	$\overline{MR}$ Input to Any Output		26	37		26	37	ns	Fig. 4	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS	
		LS196			LS197					
		MIN	TYP	MAX	MIN	TYP	MAX			
t_W	$\overline{CP_0}$ Pulse Width	12			10			ns	Fig. 1	V_{CC} = 5.0 V
t_W	$\overline{CP_1}$ Pulse Width	24			20			ns		
t_W	$\overline{PL}$ Pulse Width	18			18			ns	Fig. 3	
t_W	$\overline{MR}$ Pulse Width	12			12			ns	Fig. 4	
t_sL	Set-up Time LOW Data to $\overline{PL}$	12			12			ns	Fig. 5	
t_hL	Hold Time LOW Data to $\overline{PL}$	6.0			6.0			ns		
t_sH	Set-up Time HIGH Data to $\overline{PL}$	8.0			8.0			ns		
t_hH	Hold Time HIGH Data to $\overline{PL}$	0			0			ns		
t_{rec}	Recovery Time $\overline{PL}$ to $\overline{CP}$	16			16			ns	Fig. 4	
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP}$	18			18			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

RECOVERY TIME (t_{rec}) – is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer LOW Data to the Q outputs.

AC WAVEFORMS

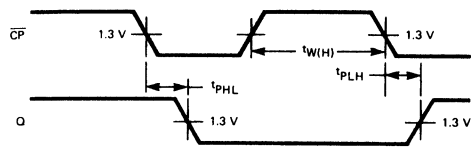
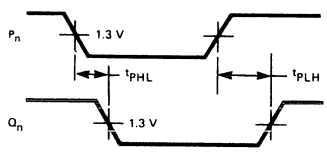


Fig. 1



NOTE: $\overline{PL}$ = LOW

Fig. 2

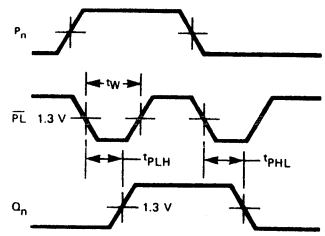


Fig. 3

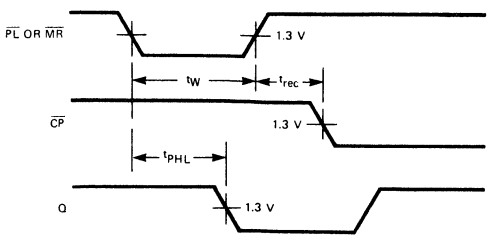
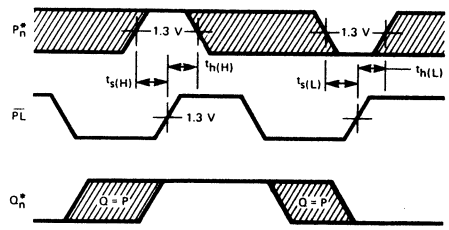


Fig. 4



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5

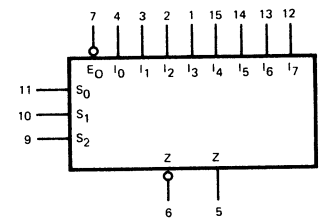
SN54LS251/SN74LS251

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION – The TTL/MSI SN54LS251/SN74LS251 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

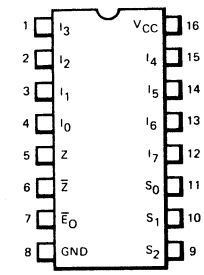
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- INVERTING AND NON-INVERTING 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



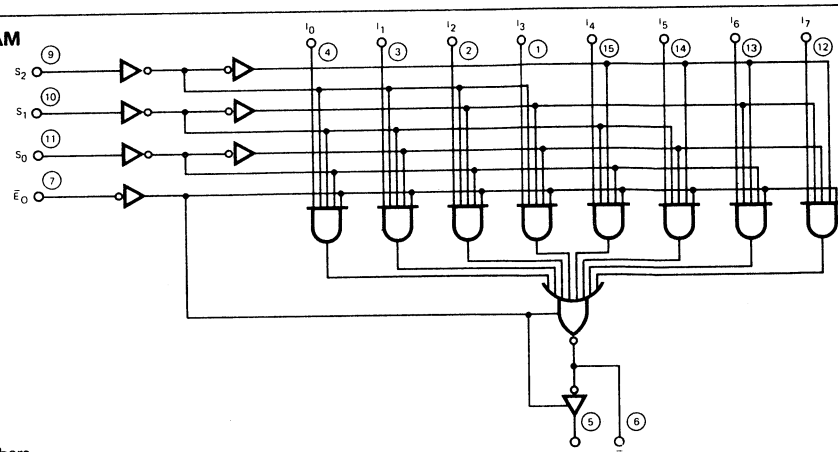
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$S_0 - S_2$	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_0 - I_7$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output (Note b)	65 (25) U.L.	5 (2.5) U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	65 (25) U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The LS251 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{E}_O$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{E}_O \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

$\overline{E}_0$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (Off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS251X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS251X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{SC}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs LOW			6.1	10	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs Off			7.1	12	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Select to $\overline{Z}$ Output		11 23	20 33	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Z Output		30 18	45 30	ns	Fig. 2	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Z}$ Output		7.0 10	12 15	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data to Z Output		18 15	27 23	ns	Fig. 2	
t_{PZH}	Output Enable Time to HIGH Level		12	20	ns	Figs. 4, 5	C_L = 15 pF R_L = 2 kΩ
t_{PZL}	Output Enable Time to LOW Level		17	25	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		12	20	ns	Figs. 3, 5	C_L = 5 pF R_L = 2 kΩ
t_{PHZ}	Output Disable Time from HIGH Level		17	25	ns	Figs. 4, 5	

3-STATE AC WAVEFORMS

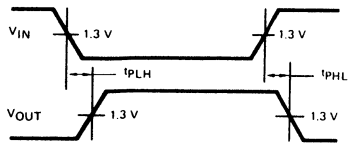


Fig. 1

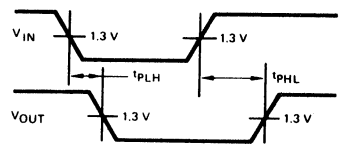


Fig. 2

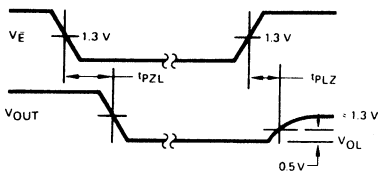


Fig. 3

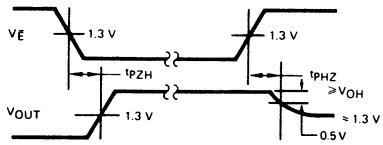
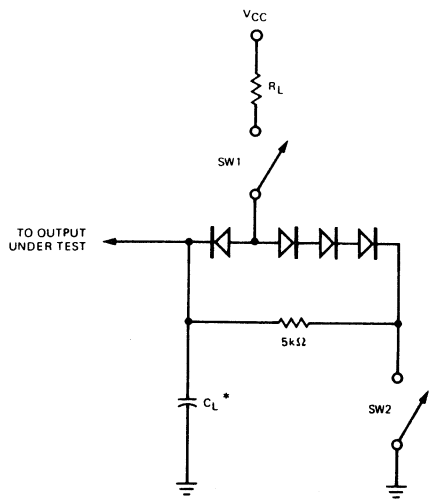


Fig. 4

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

SN54LS253/SN74LS253

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

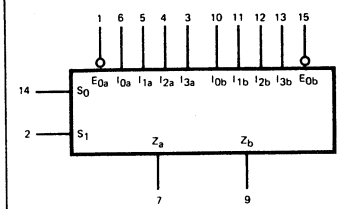
DESCRIPTION — The LSTTL/MSI SN54LS253/SN74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_O) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES		LOADING (Note a) HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
$\overline{E}_{0a}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_a	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.
Multiplexer B			
$\overline{E}_{0b}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_b	Multiplexer Output (Note b)	65(25) U.L.	5(2.5) U.L.

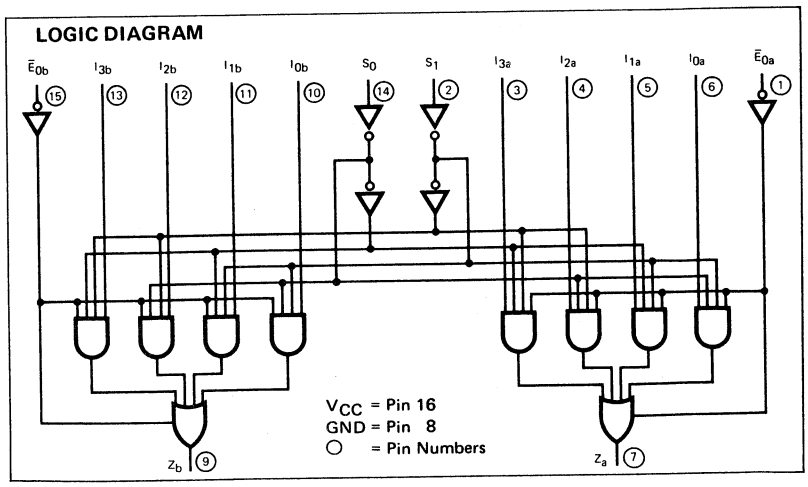
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

LOGIC SYMBOL

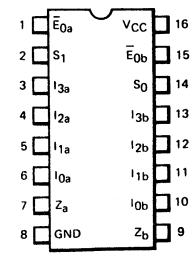


V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_{0a} \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_{0b} \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{E}_0$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level
L = LOW Level
X = Irrelevant
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS253X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS253X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1			I_{OH} = −2.6 mA
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, $V_{\overline{E}}$ = 2.0 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current, Outputs LOW			7.0	12	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V
	Power Supply Current, Outputs Off			8.5	14		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C (See Page 5-98 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		10 10	15 15	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		20 16	29 24	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level		12	18	ns	Figs. 4, 5	C_L = 15 pF, R_L = 2 kΩ
t_{PZL}	Output Enable Time to LOW Level		11	18	ns	Figs. 3, 5	
t_{PLZ}	Output Disable Time from LOW Level		22	32	ns	Figs. 3, 5	C_L = 5 pF, R_L = 2 kΩ
t_{PHZ}	Output Disable Time from HIGH Level		11	18	ns	Figs. 4, 5	

SN54LS257/SN74LS257

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The LSTTL/MSI SN54LS257/SN74LS257 is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{E}_O$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

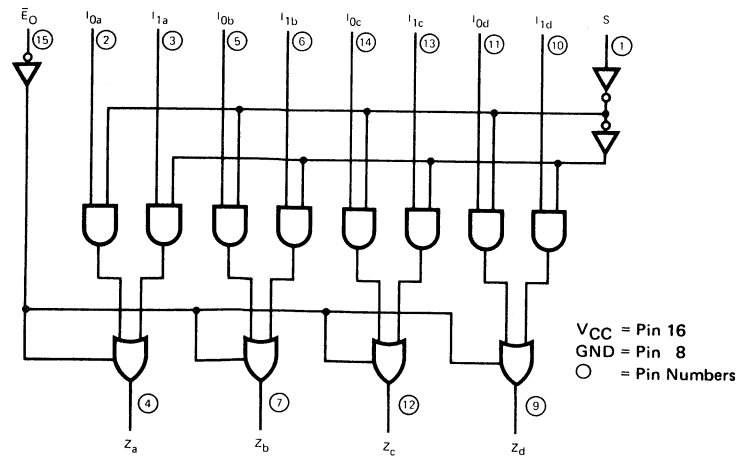
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

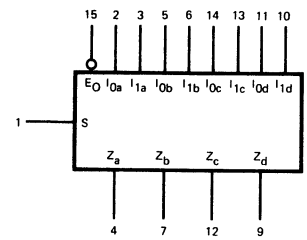
		LOADING (Note a) HIGH	LOW
S	Common Data Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$Z_a - Z_d$	Multiplexer Outputs (Note b)	65(25) U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

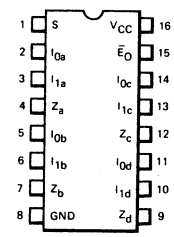


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS257 is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select Input. When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form.

The LS257 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E}_O \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = \overline{E}_O \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{E}_O \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = \overline{E}_O \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}_O$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance (off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS257X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS257X	4.75 V	5.0 V	5.25 V	0°C to + 75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current $\overline{E}_0$, I_{0x}, I_{1x}				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	S				40			
	Input HIGH Current at MAX Input Voltage $\overline{E}_0$, I_{0x}, I_{1x}				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
	S				0.2			
I_{IL}	Input LOW Current $\overline{E}_0$, I_{0x}, I_{1x}				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	S				−0.8			
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs HIGH				10	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs LOW				16		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs OFF				17		V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 5-98 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			18 14	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output			21 21	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level			28	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level			24	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level			22	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			14	ns	Figs. 4, 5	R_L = 2 kΩ

SN54LS258/SN74LS258

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION — The LSTTL/MSI SN54LS258/SN74LS258 is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{E}_O$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

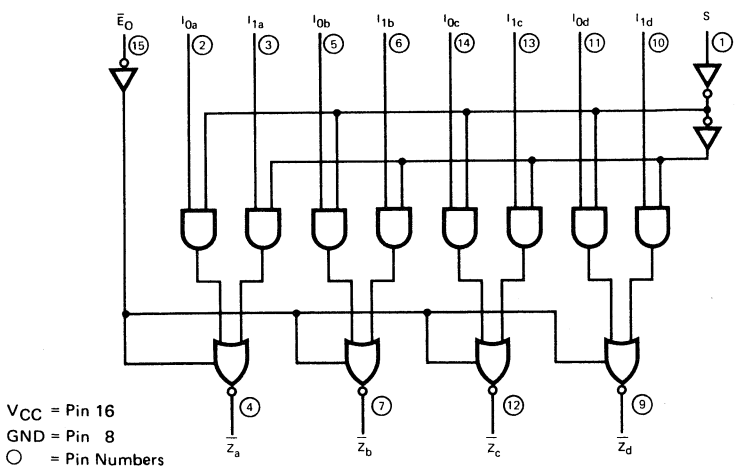
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
S	Common Select Input	1.0 U.L.	0.5 U.L.
$\overline{E}_O$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
$\overline{Z}_a - \overline{Z}_d$	Multiplexer Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

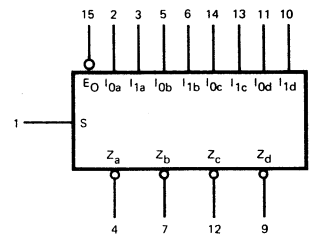
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



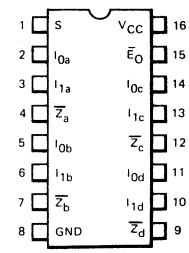
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS258 is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select Input (S). When the Select Input is LOW, the I_0 inputs are selected and when Select is HIGH, the I_1 inputs are selected. The data on the selected inputs appears at the outputs in inverted form.

The LS258 Quad 2-Input Multiplexer is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E}_O \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad \overline{Z}_b = \overline{E}_O \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Z}_c = \overline{E}_O \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad \overline{Z}_d = \overline{E}_O \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable Input ($\overline{E}_O$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}_O$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High Impedance (Off)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS258X	4.5 V	5.0 V	5.5 V	–55°C to +125°C
SN74LS258X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current $\overline{E}_0$, I_{0x}, I_{1x}				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	S				40			
	Input HIGH Current at MAX Input Voltage $\overline{E}_0$, I_{0x}, I_{1x}				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
	S				0.2			
I_{IL}	Input LOW Current $\overline{E}_0$, I_{0x}, I_{1x}				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	S				−0.8			
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs HIGH				9.0	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs LOW				11	mA	V_{CC} = MAX, V_{IN} = 4.5 V, $V_{\overline{E}}$ = 0 V	
	Power Supply Current, Outputs OFF				12	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See Page 5-98 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			14 14	ns	Fig. 1	C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Select to Output			21 21	ns	Fig. 1	C_L = 15 pF
t_{PZH}	Output Enable Time to HIGH Level			30	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level			16	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			16	ns	Figs. 4, 5	R_L = 2 kΩ

SN54LS259/SN74LS259

8-BIT ADDRESSABLE LATCH

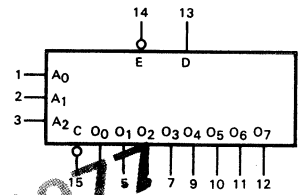
DESCRIPTION — The SN54LS259/SN74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable.

- **SERIAL-TO-PARALLEL CONVERSION**
- **8-BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **FULLY TTL COMPATIBLE**

PIN NAMES

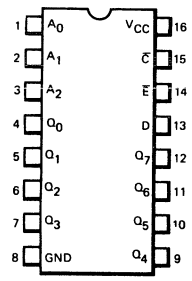
A_0, A_1, A_2	Address Inputs
D	Data Input
$\overline{E}$	Enable (Active LOW) Input
$\overline{C}$	Clear (Active LOW) Input
Q_0 to Q_7	Parallel Latch Outputs

LOGIC SYMBOL

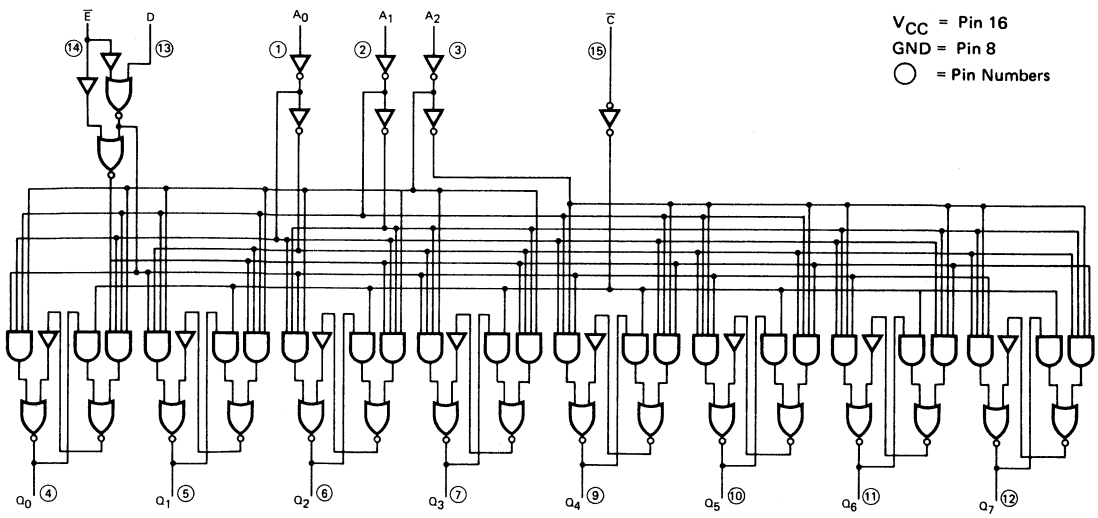


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

SN54LS283/SN74LS283

4-BIT BINARY FULL ADDER WITH FAST CARRY

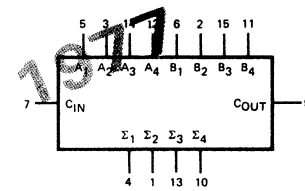
DESCRIPTION — The SN54LS283/SN74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ($A_1 - A_4$, $B_1 - B_4$) and a Carry Input (C_{IN}). It generates the binary Sum outputs ($\Sigma_1 - \Sigma_4$) and the Carry Output (C_{OUT}) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

PIN NAMES

		LOADING (Note a) HIGH	LOW
$A_1 - A_4$	Operand A Inputs	1.0 U.L.	0.5 U.L.
$B_1 - B_4$	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_{IN}	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1 - \Sigma_4$	Sum Outputs (Note b)	10 U.L.	5(2.5) U.L.
C_{OUT}	Carry Output (Note b)	10 U.L.	5(2.5) U.L.

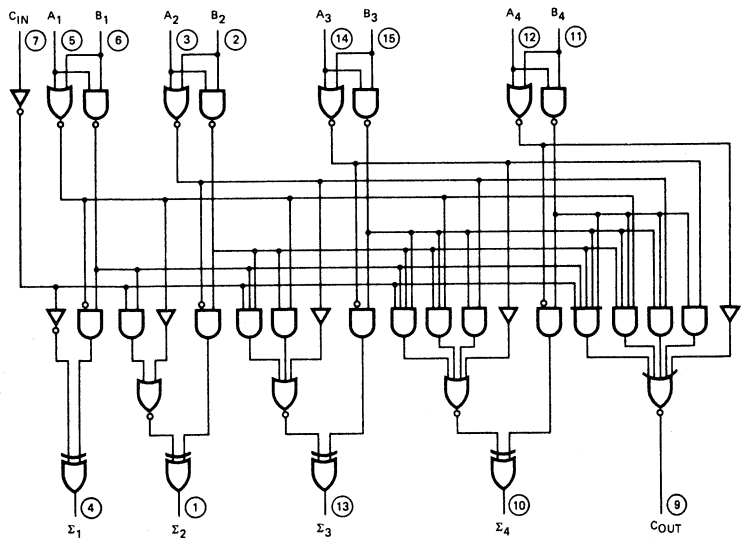
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



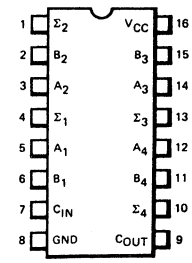
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_{OUT}) outputs.

$$C_{IN}+(A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_{OUT}$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1, can be arbitrarity assigned to pins 7, 5 or 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS283X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS283X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current C_{IN} Any A or B				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	C_{IN} Any A or B				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current C_{IN} Any A or B				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			22	39	mA	V_{CC} = MAX, All Inputs = 0 V
				19	34	mA	V_{CC} = MAX, A Inputs = 4.5 V

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to Any Σ Output			24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs			24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_{IN} Input to C_{OUT} Output			17 17	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_{OUT} Output			17 17	ns	

AC WAVEFORMS

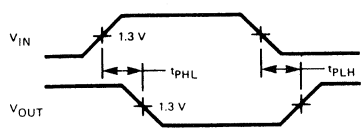


Fig. 1

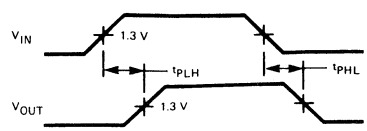


Fig. 2

SN54LS290/SN74LS290

DECADE COUNTER

SN54LS293/SN74LS293

4-BIT BINARY COUNTER

DESCRIPTION — The SN54LS290/SN74LS290 and SN54LS293/SN74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

- **CORNER POWER PIN VERSIONS OF THE LS90 and LS93.**
- **LOW POWER CONSUMPTION .... TYPICALLY 45 mW**
- **HIGH COUNT RATES .... TYPICALLY 50 MHz**
- **CHOICE OF COUNTING MODES .... BCD, BI-QUINARY, BINARY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section.	3.0 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS290).	2.0 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS293).	1.0 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS290) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 & ÷8 Sections (Note b)	10 U.L.	5(2.5) U.L.

NOTES:

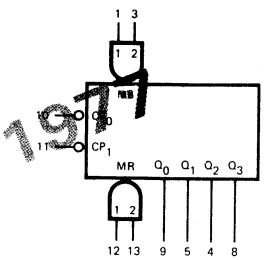
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ Input of the device.

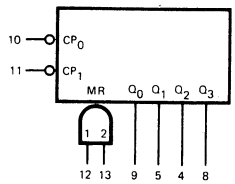
LOGIC SYMBOL

LS290



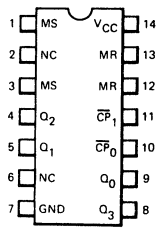
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 6

LS293



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 1, 2, 3, 6

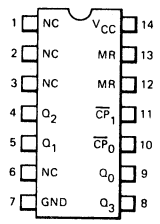
CONNECTION DIAGRAM **LS290**
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NC — No Internal Connection

CONNECTION DIAGRAM **LS293**
DIP (TOP VIEW)

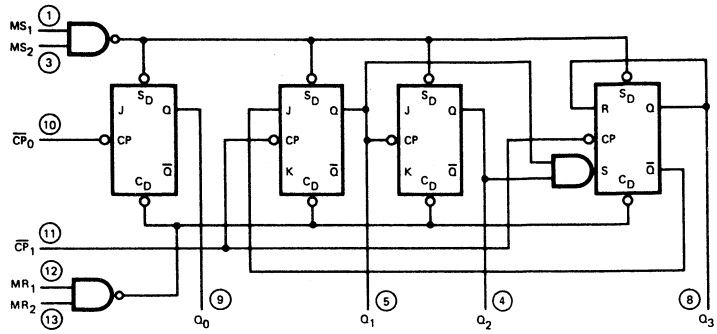


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

NC — No internal connection

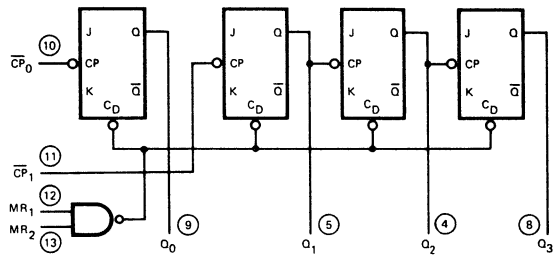
LOGIC DIAGRAMS

LS290



○ = Pin Numbers
V_{CC} = Pin 14
GND = 7

LS293



○ = Pin Numbers
V_{CC} = Pin 14
GND = 7

FUNCTIONAL DESCRIPTION – The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

LS290

A. BCD Decade (8421) Counter – the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter – The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter – No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS293

A. 4-Bit Ripple Counter – The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous division of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter – The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS290 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

LS293 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

LS290
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS293
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input CP_1.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	TEMPERATURE
SN54LS290X SN54LS293X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS290X SN74LS293X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS290) $\overline{CP}_1$ (LS293)				20 120 80 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	MS, MR $\overline{CP}_0$, $\overline{CP}_1$ (LS293) $\overline{CP}_1$ (LS290)				0.1 0.4 0.8	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS290) $\overline{CP}_1$ (LS293)				−0.4 −2.4 −3.2 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			9	15	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS	
		LS290		LS293				
		MIN	MAX	MIN	MAX			
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		MHz	Fig. 1	
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		MHz	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18	ns	Fig. 1	$V_{CC} = 5.0$ V $C_L = 15$ pF
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_1 Output		16 21		16 21	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_2 Output		32 35		32 35	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_3 Output		32 35		51 51	ns		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_3 Output		48 50		70 70	ns		
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		30			ns	Fig. 3	
t_{PHL}	MS Input to Q_1 and Q_2Outputs		40			ns	Fig. 2	
t_{PHL}	MR Input to Any Output		40		40	ns	Fig. 2	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS	
		LS290		LS293				
		MIN	MAX	MIN	MAX			
t_W	$\overline{CP}_0$ Pulse Width	15		15		ns	Fig. 1	$V_{CC} = 5.0$ V
t_W	$\overline{CP}_1$ Pulse Width	30		30		ns		
t_W	MS Pulse Width	15				ns	Fig. 2, 3	
t_W	MR Pulse Width	15		15		ns	Fig. 2	
t_{rec}	Recovery Time MS to $\overline{CP}$	25				ns	Fig. 2, 3	
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		ns	Fig. 2	

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

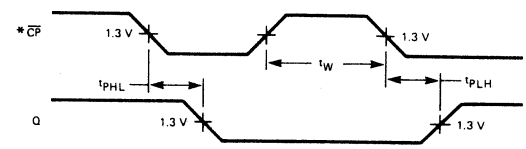


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

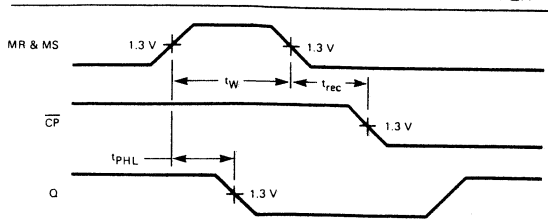


Fig. 2

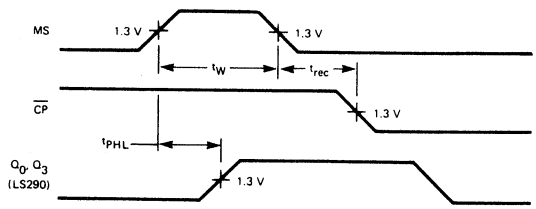


Fig. 3

SN54LS295A/SN74LS295A

4-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

DESCRIPTION – The SN54LS295A/SN74LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes, and independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (EO). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion.

The LS295 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

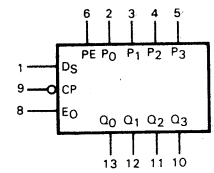
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **NEGATIVE EDGE-TRIGGERED CLOCK INPUT**
- **PARALLEL ENABLE MODE CONTROL INPUT**
- **3-STATE BUSSABLE OUTPUT BUFFERS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
PE	Parallel Enable Input	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$P_0 - P_3$	Parallel Data Input	0.5 U.L.	0.25 U.L.
E_O	Output Enable Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock Pulse (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	3-State Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

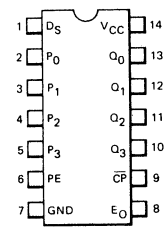
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



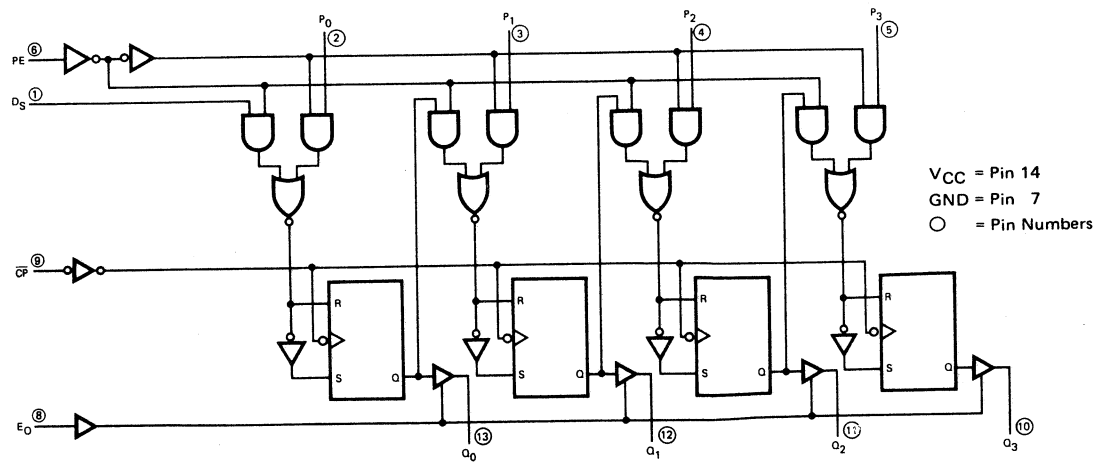
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The LS295 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data ($P_0 - P_3$) inputs and four parallel 3-State output buffers ($Q_0 - Q_3$). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data Inputs ($P_0 - P_3$) into the register synchronous with the HIGH to LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH to LOW transition on the clock transfers the serial data on the D_S input to register Q_0, and shifts data from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. The input data and parallel enable are fully edge-triggered and must be stable only one set-up time before the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (E_O). When the E_O is HIGH, the four register outputs appear at the $Q_0 - Q_3$ outputs. When E_O is LOW, the outputs are forced to a high impedance "off" state. The 3-State output buffers are completely independent of the register operation, i.e., the input transitions on the E_O input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-State devices whose outputs are tied together are designed so there is no overlap.

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS*			
	PE	$\overline{CP}$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift Right	l	⌐	l	X	L	q_0	q_1	q_2
	l	⌐	h	X	H	q_0	q_1	q_2
Parallel Load	h	⌐	X	P_n	P_0	P_1	P_2	P_3

*The indicated data appears at the Q outputs when E_O is HIGH. When E_O is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance "off" state.

L = LOW Voltage Levels
H = HIGH Voltage Levels
X = Don't Care

$p_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +15 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS295AX	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS295AX	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.4			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Output Off Current LOW				20	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs HIGH			14	23	mA	V_{CC} = MAX, V_{CP} = ⎍, V_E = 4.5 V	
	Power Supply Current, Outputs Off			15	25	mA	V_{CC} = MAX, V_{CP} = 0 V, V_E = 0 V	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
f_{MAX}	Shift Frequency	30	45		MHz	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		17 17	26 26	ns	Fig. 1	

AC CHARACTERISTICS: for 3-State Output Buffers (See Page 5-98 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PZH}	Output Enable Time to HIGH Level		12	18	ns	Figs. 4, 5	C_L = 15 pF
t_{PZL}	Output Enable Time to LOW Level		12	18	ns	Figs. 3, 5	R_L = 2 kΩ
t_{PLZ}	Output Disable Time from LOW Level		12	18	ns	Figs. 3, 5	C_L = 5 pF
t_{PHZ}	Output Disable Time from HIGH Level		12	18	ns	Figs. 4, 5	R_L = 2 kΩ

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_W(CP)	Clock Pulse Width	20			ns	Fig. 1	
t_s(Data)	Set-up Time, Data to Clock	20			ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_h(Data)	Hold Time, Data to Clock	0			ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_s(PE)	Set-up Time, PE to Clock	20			ns	Fig. 2	V_{CC} = 5.0 V, C_L = 15 pF
t_h(PE)	Hold Time, PE to Clock	0			ns	Fig. 2	V_{CC} = 5.0 V, C_L = 15 pF

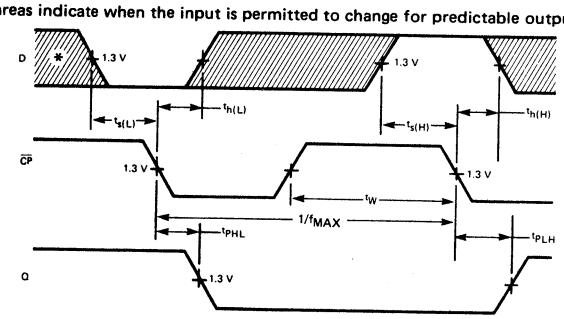
DEFINITION OF TERMS

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for PE = LOW and P_n for PE = HIGH.

Fig. 1

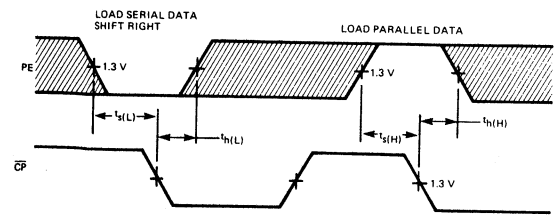


Fig. 2

SN54LS298/SN74LS298

QUAD 2-PORT REGISTER
(QUAD 2-INPUT MULTIPLEXER WITH STORAGE)

DESCRIPTION — The SN54LS298/SN74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

The LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all Motorola TTL families.

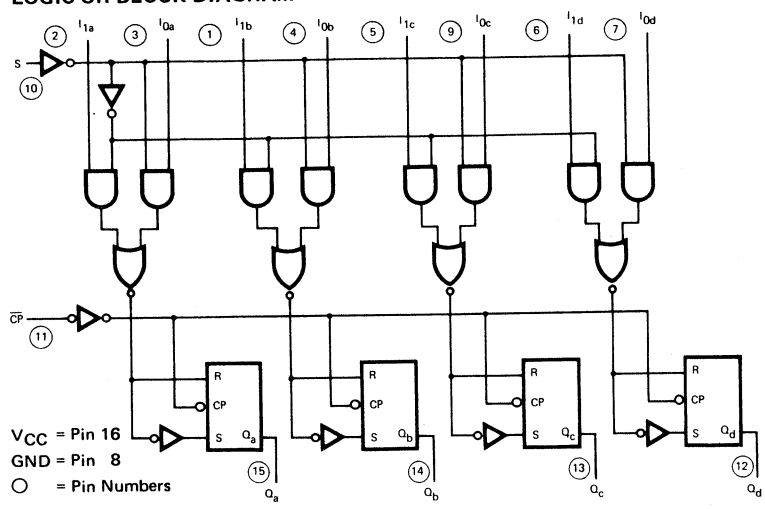
- **SELECT FROM TWO DATA SOURCES**
- **FULLY EDGE-TRIGGERED OPERATION**
- **TYPICAL POWER DISSIPATION OF 65 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PIN NAMES

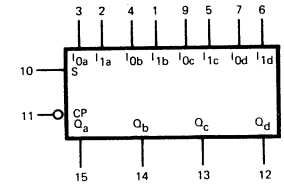
		LOADING (Note a) HIGH	LOW
S	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active LOW Going Edge) Input	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{0d}$	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
$I_{1a} - I_{1d}$	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
$Q_a - Q_d$	Register Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC OR BLOCK DIAGRAM

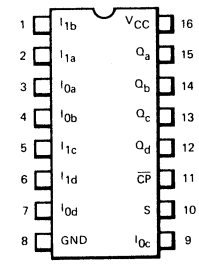


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one set-up time prior to the HIGH to LOW transition of the clock for predictable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS298X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS298X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			13	21	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		16 16	25 25	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
$t_{W(H)}$	Clock Pulse Width (HIGH)	20			ns	Fig. 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clock Pulse Width (LOW)	20			ns		
$t_{s(Data)}$	Set-up Time, Data to Clock	15			ns	Fig. 1	
$t_{h(Data)}$	Hold Time, Data to Clock	5.0			ns		
$t_{s(S)}$	Set-up Time, Select to Clock	20			ns	Fig. 2	
$t_{h(S)}$	Hold Time, Select to Clock	0			ns		

DEFINITIONS OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

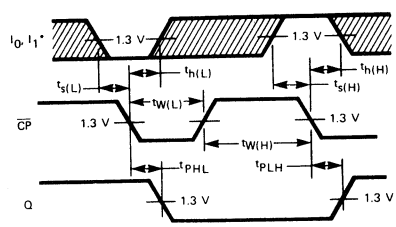


Fig. 1

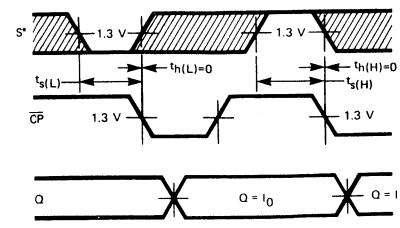


Fig. 2

*The shaded areas indicate when the input is permitted to change for predictable output performance.

SN54LS670/SN74LS670

4×4 REGISTER FILE WITH 3-STATE OUTPUTS

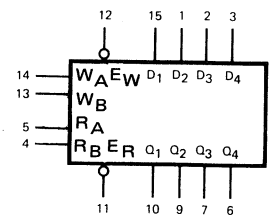
DESCRIPTION — The TTL/MSI SN54LS670/SN74LS670 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54LS170/SN74LS170 provides a similar function to this device but it features open-collector outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS BY n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **3-STATE OUTPUTS FOR EXPANSION**
- **TYPICAL POWER DISSIPATION OF 125 mW**

LOGIC SYMBOL



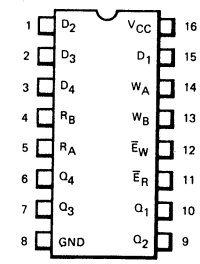
V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

		LOADING (Note a) HIGH	LOW
D_1-D_4	Data Inputs	0.5 U.L.	0.25 U.L.
W_A, W_B	Write Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_W$	Write Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
R_A, R_B	Read Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_R$	Read Enable (Active LOW) Input	1.5 U.L.	0.75 U.L.
Q_1-Q_4	Outputs (Note b)	65(25) U.L.	5(2.5) U.L.

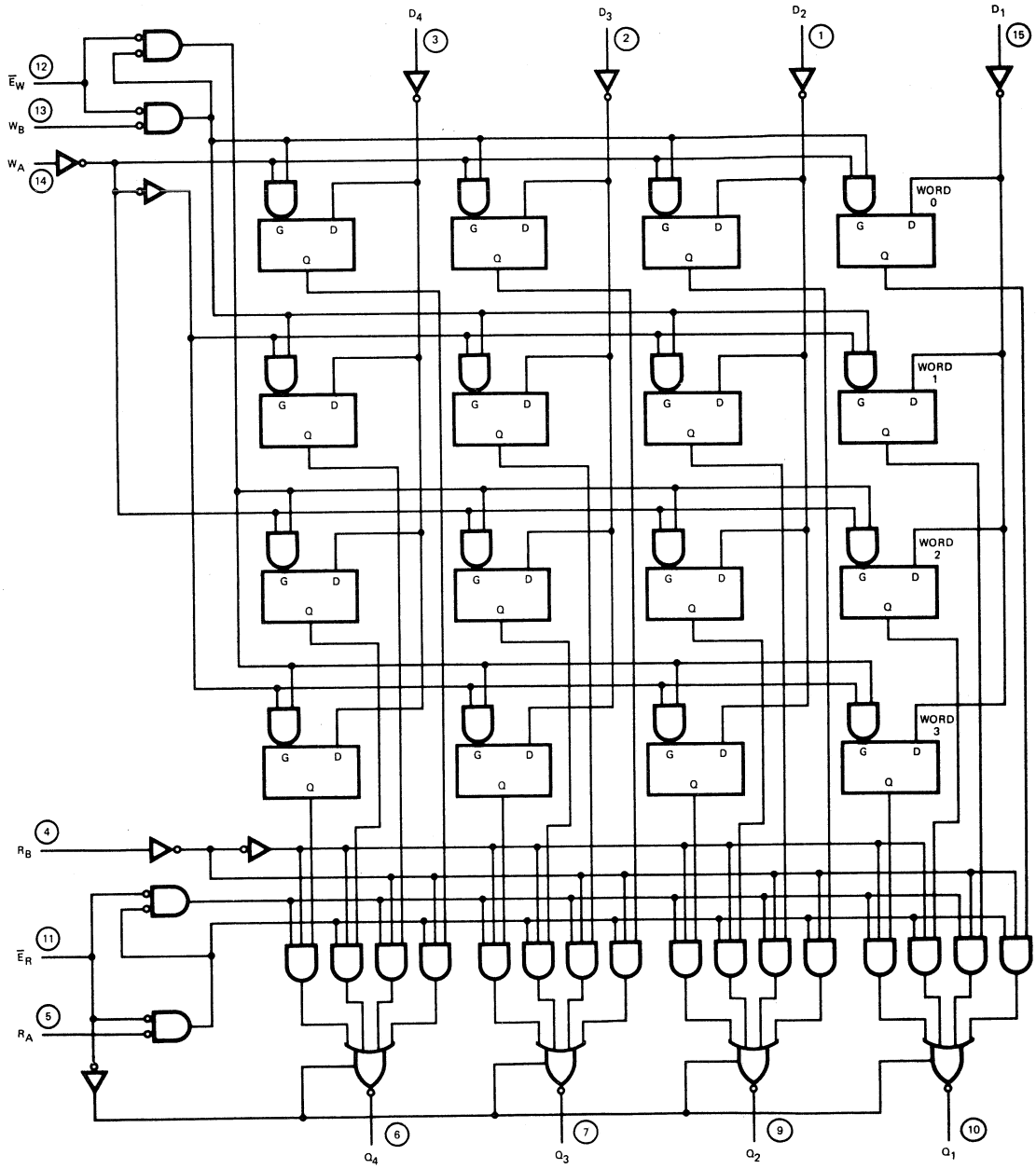
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5.0 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



○ = Pin Numbers
V_{CC} = Pin 16
GND = Pin 8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +10 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS670X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS670X	4.75 V	5.0 V	5.25 V	0°C to +75°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTIC OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V, V_{IH} = 2 V
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_{IH} = 2 V
I_{IH}	Input HIGH Current Any D, R or W $\overline{E}_W$ $\overline{E}_R$				20 40 60	μA	V_{CC} = MAX, V_{IN} 2.7 V
	Any D, R or W $\overline{E}_W$ $\overline{E}_R$				0.1 0.2 0.3	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current Any D, R or W $\overline{E}_W$ $\overline{E}_R$				−0.4 −0.8 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			30	50	mA	V_{CC} = MAX (Note 5)

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.
5. Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay R_A or R_B to Q Outputs			40 45	ns	Fig. 2	$V_{CC} = 5$ V $C_L = 15$ pF $R_L = 2$ kΩ
t_{PLH} t_{PHL}	Propagation Delay, Negative Going $\overline{E}_W$ to Q Outputs			45 50	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs			45 40	ns	Fig. 1	
t_{PZH}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going HIGH			35	ns	Fig. 4,5	$V_{CC} = 5$ V $C_L = 5.0$ pF $R_L = 2$ kΩ See Page 5-98 for 3-state Waveforms (Figs. 3,4,5)
t_{PZL}	Enable Time, Negative Going $\overline{E}_R$ to Q Outputs Going LOW			40	ns	Fig. 3,5	
t_{PHZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from HIGH			50	ns	Fig. 4,5	
t_{PLZ}	Disable Time, Positive Going $\overline{E}_R$ to Q Outputs Off from LOW			35	ns	Fig. 3,5	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_W	Pulse Width (LOW) for $\overline{E}_W$	25			ns	$V_{CC} = 5$ V Fig. 6 (Note 9)
t_sD (Note 6)	Set-Up Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	10			ns	
t_hD	Hold Time, Data Inputs with Respect to Positive-Going $\overline{E}_W$	15			ns	
t_sW (Note 8)	Set-Up Time, Write Select Inputs W_A and W_B with Respect to Negative-Going $\overline{E}_W$	15			ns	
t_hW	Hold Time, Write Select Inputs W_A and W_B with Respect to Positive-Going $\overline{E}_W$	5			ns	

NOTES:

6. The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.
7. The Hold Time (t_h) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.
8. The Address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
9. The shaded areas indicate when the input are permitted to change for predictable output performance.

AC WAVEFORMS

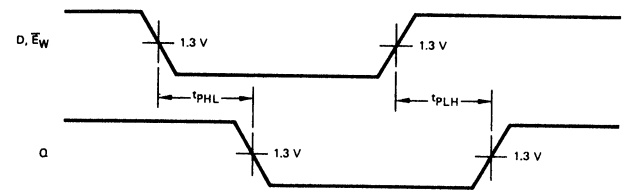


Fig. 1

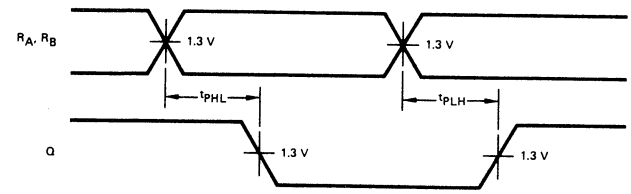


Fig. 2

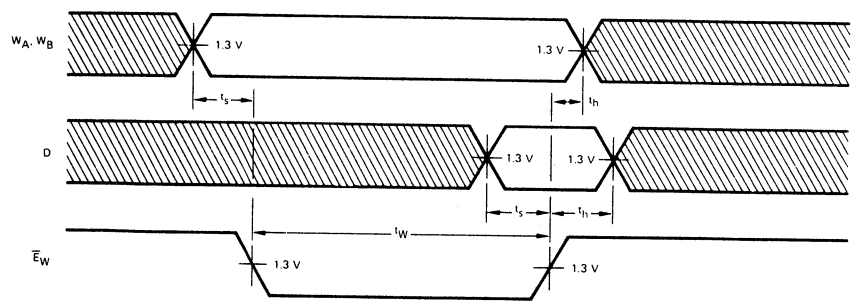
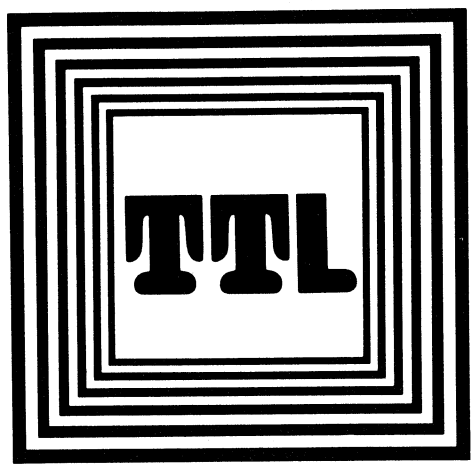


Fig. 6

LOW POWER SCHOTTKY



Ordering Information and Package Outlines

6

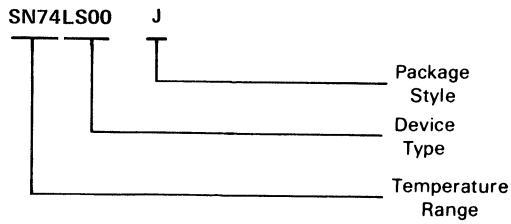
LOW POWER SCHOTTKY ORDERING INFORMATION

TEMPERATURE RANGE

54LS = Military $-55^{\circ}C$ to $+125^{\circ}C$
74LS = Commercial $0^{\circ}C$ to $+75^{\circ}C$

PACKAGE STYLE

J = Dual In-Line — Ceramic (Hermetic)
N = Dual In-Line — Plastic
W = Flat Package



In order to accommodate varying die sizes (SSI, MSI, etc.), numbers of pins (14, 16, 24, etc.), and package outlines, a number of different package forms are required in each of the three package style categories.

The following lists indicate the specific package dimensions currently used for each device type. The detailed outline corresponding to each package code is shown at the end of this section.

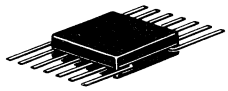
DEVICE	MILITARY (54LS) $-55^{\circ}C$ to $+125^{\circ}C$		DEVICE	COMMERCIAL (74LS)/INDUSTRIAL $0^{\circ}C$ to $+75^{\circ}C$		
	CERAMIC DIP (J)	FLATPAK (W)		CERAMIC DIP (J)	PLASTIC DIP (N)	FLATPAK (W)
54LS00	632-02	607-04	74LS00	632-02	646	607-04
54LS02	632-02	607-04	74LS02	632-02	646	607-04
54LS03	632-02	607-04	74LS03	632-02	646	607-04
54LS04	632-02	607-04	74LS04	632-02	646	607-04
54LS05	632-02	607-04	74LS05	632-02	646	607-04
54LS08	632-02	607-04	74LS08	632-02	646	607-04
54LS09	632-02	607-04	74LS09	632-02	646	607-04
54LS10	632-02	607-04	74LS10	632-02	646	607-04
54LS11	632-02	607-04	74LS11	632-02	646	607-04
54LS14	632-02	607-04	74LS14	632-02	646	607-04
54LS15	632-02	607-04	74LS15	632-02	646	607-04
54LS20	632-02	607-04	74LS20	632-02	646	607-04
54LS21	632-02	607-04	74LS21	632-02	646	607-04
54LS22	632-02	607-04	74LS22	632-02	646	607-04
54LS27	632-02	607-04	74LS27	632-02	646	607-04

DEVICE	MILITARY (54LS) −55°C to +125°C		DEVICE	COMMERCIAL (74LS)/INDUSTRIAL 0°C to +75°C		
	CERAMIC DIP (J)	FLATPAK (W)		CERAMIC DIP (J)	PLASTIC DIP (N)	FLATPAK (W)
54LS30	632-02	607-04	74LS30	632-02	646	607-04
54LS32	632-02	607-04	74LS32	632-02	646	607-04
54LS37	632-02	607-04	74LS37	632-02	646	607-04
54LS38	632-02	607-04	74LS38	632-02	646	607-04
54LS40	632-02	607-04	74LS40	632-02	646	607-04
54LS42	620	650	74LS42	620	648	650
54LS51	632-02	607-04	74LS51	632-02	646	607-04
54LS54	632-02	607-04	74LS54	632-02	646	607-04
54LS55	632-02	607-04	74LS55	632-02	646	607-04
54LS73	632-02	607-04	74LS73	632-02	646	607-04
54LS74	632-02	607-04	74LS74	632-02	646	607-04
54LS83	620	650	74LS83	620	648	650
54LS86	632-02	607-04	74LS86	632-02	646	607-04
54LS90	632-02	607-04	74LS90	632-02	646	607-04
54LS92	632-02	607-04	74LS92	632-02	646	607-04
54LS93	632-02	607-04	74LS93	632-02	646	607-04
54LS95	632-02	607-04	74LS95	632-02	646	607-04
54LS109	620	650	74LS109	620	648	650
54LS112	620	650	74LS112	620	648	650
54LS113	632-02	607-04	74LS113	632-02	646	607-04
54LS114	632-02	607-04	74LS114	632-02	646	607-04
54LS125	632-02	607-04	74LS125	632-02	646	607-04
54LS126	632-02	607-04	74LS126	632-02	646	607-04
54LS132	632-02	607-04	74LS132	632-02	646	607-04
54LS133	620	650	74LS133	620	648	650
54LS136	632-02	607-04	74LS136	632-02	646	607-04
54LS138	620	650	74LS138	620	648	650
54LS139	620	650	74LS139	620	648	650
54LS151	620	650	74LS151	620	648	650
54LS152	632-02	607-04	74LS152	632-02	646	607-04
54LS153	620	650	74LS153	620	648	650
54LS155	620	650	74LS155	620	648	650
54LS156	620	650	74LS156	620	648	650
54LS157	620	650	74LS157	620	648	650
54LS158	620	650	74LS158	620	648	650
54LS160	620	650	74LS160	620	648	650
54LS161	620	650	74LS161	620	648	650
54LS162	620	650	74LS162	620	648	650
54LS163	620	650	74LS163	620	648	650
54LS164	632-02	607-04	74LS164	632-02	646	607-04
54LS170	620	650	74LS170	620	648	650
54LS174	620	650	74LS174	620	648	650
54LS175	620	650	74LS175	620	648	650
54LS181	623	652	74LS181	623	649	652
54LS190	620	650	74LS190	620	648	650

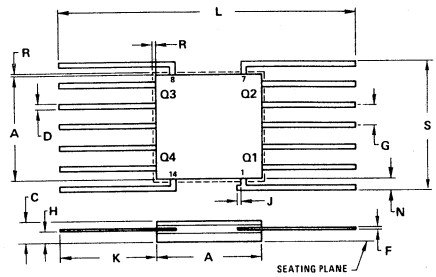
DEVICE	MILITARY (54LS) −55°C to +125°C		DEVICE	COMMERCIAL (74LS)/INDUSTRIAL 0°C to +75°C		
	CERAMIC DIP (J)	FLATPAK (W)		CERAMIC DIP (J)	PLASTIC DIP (N)	FLATPAK (W)
54LS191	620	650	74LS191	620	648	650
54LS192	620	650	74LS192	620	648	650
54LS193	620	650	74LS193	620	648	650
54LS194	620	650	74LS194	620	648	650
54LS195	620	650	74LS195	620	648	650
54LS196	632-02	607-04	74LS196	632-02	646	607-04
54LS197	632-02	607-04	74LS197	632-02	646	607-04
54LS251	620	650	74LS251	620	648	650
54LS253	620	650	74LS253	620	648	650
54LS257	620	650	74LS257	620	648	650
53LS258	620	650	74LS258	620	648	650
54LS259	620	650	74LS259	620	648	650
54LS266	632-02	607-04	74LS266	632-02	646	607-04
54LS279	620	650	74LS279	620	648	650
54LS283	620	650	74LS283	620	648	650
54LS290	632-02	607-04	74LS290	632-02	646	607-04
54LS293	632-02	607-04	74LS293	632-02	646	607-04
54LS295	632-02	607-04	74LS295	632-02	646	607-04
54LS298	620	650	74LS298	620	648	650
54LS365	620	650	74LS365	620	648	650
54LS366	620	650	74LS366	620	648	650
54LS367	620	650	74LS367	620	648	650
54LS368	620	650	74LS368	620	648	650
54LS670	620	650	74LS670	620	648	650

PACKAGE OUTLINES

Case 607-04
14-Pin Ceramic



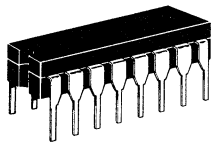
STYLE 1:
PIN
Q1 { 1. COLLECTOR
2. BASE
3. EMITTER
4. NOT CONNECTED
Q2 { 5. EMITTER
6. BASE
7. COLLECTOR
Q3 { 8. COLLECTOR
9. BASE
10. EMITTER
11. NOT CONNECTED
Q4 { 12. EMITTER
13. BASE
14. COLLECTOR



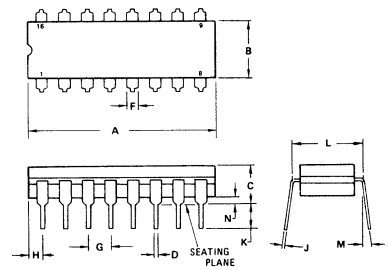
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.99	0.240	0.275
C	0.76	2.03	0.030	0.080
D	0.25	0.48	0.010	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
J	–	0.38	–	0.015
K	6.35	–	0.250	–
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

NOTE:
1. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION RELATIVE TO "A" AT MAXIMUM MATERIAL CONDITION.

Case 620
14-Pin Ceramic Dual In-Line

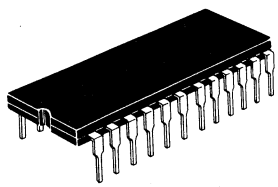


NOTES:
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2 PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

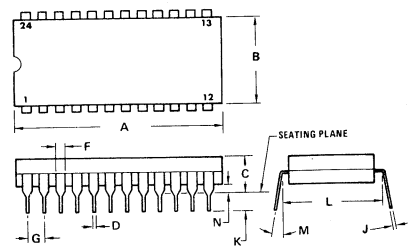


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

Case 623
24-Pin Ceramic Dual In-Line



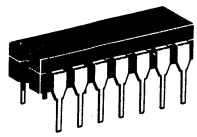
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

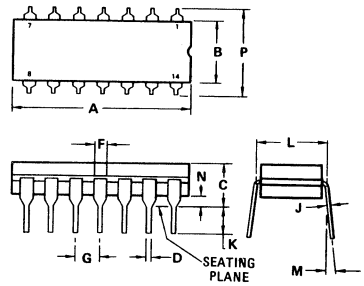


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

PACKAGE OUTLINES

Case 632-02
14-Pin Ceramic Dual In-Line

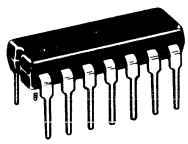




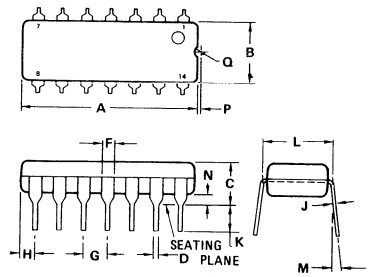
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15^0	–	15^0
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

Case 646
14-Pin Plastic Dual In-Line

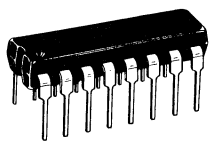


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

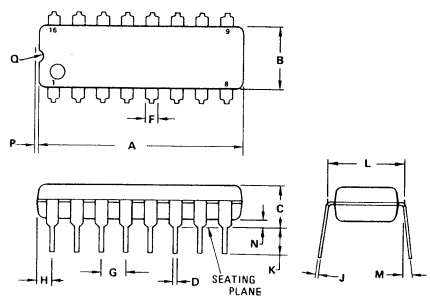


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

Case 648
16-Pin Plastic Dual In-Line



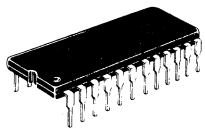
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

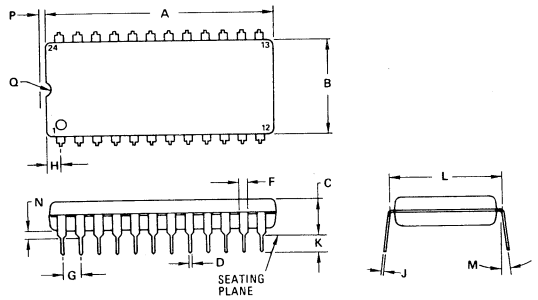


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

PACKAGE OUTLINES

Case 649
24-Pin Plastic Dual In-Line

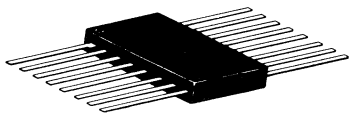


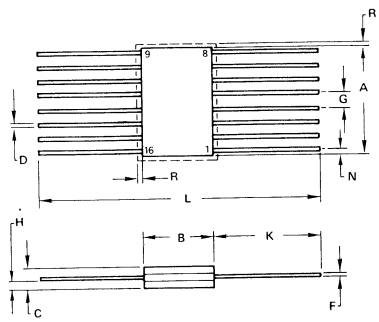


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

Case 650
16-Pin Ceramic

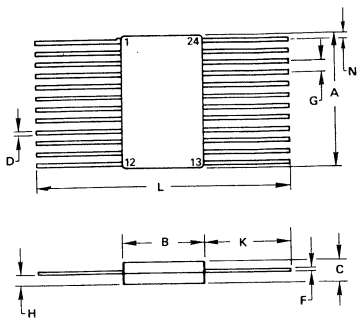




NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	6.60	0.245	0.260
C	1.52	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

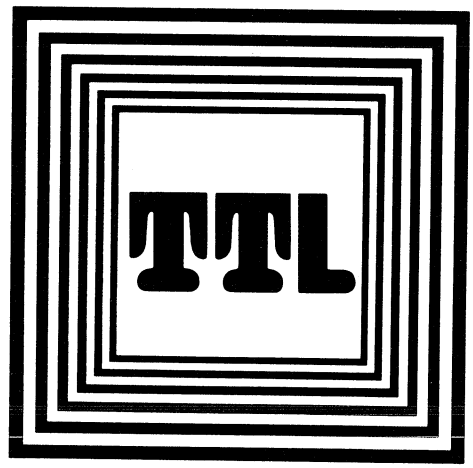
Case 652
24-Pin Ceramic



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025

LOW POWER SCHOTTKY



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